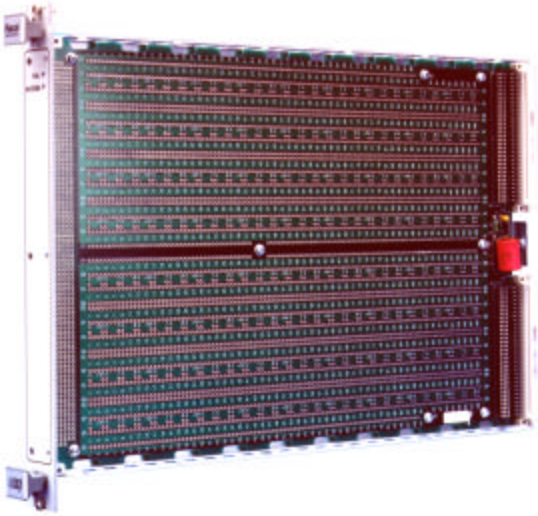
INSTRUCTION MANUAL

7064R

REGISTER BASED PROTOTYPE MODULE

PUBLICATION NO. 980817



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EC Declaration of Conformity

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declare under sole responsibility that the

7064R 1S Reg Based Prototype Module, P/N 407620-110
7064R 2S Reg Based Prototype Module, P/N 407620-210
7064R 3S Reg Based Prototype Module, P/N 407620-310

conforms to the following Product Specifications:

Safety: EN61010-1:1993+A2:1995

EMC: EN61326:1997+A1:1998,CLASS A

Supplementary Information:

The above specifications are met when the product is installed in a Racal Instruments certified mainframe with faceplates installed over all unused slots, as applicable.

The product herewith complies with the requirements of the EMC Directive 89/336/EEC (modified by 93/68/EEC EMC Directive) and 73/23/EEC (Low Voltage Directive).

Irvine, CA, March 5, 2002

Karen L Evensen

Karen Evensen
Director of Engineering

FOR YOUR SAFETY

Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNINGS** and **CAUTION** notices.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.

Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.

Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.

2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until, performance is checked by qualified personnel.

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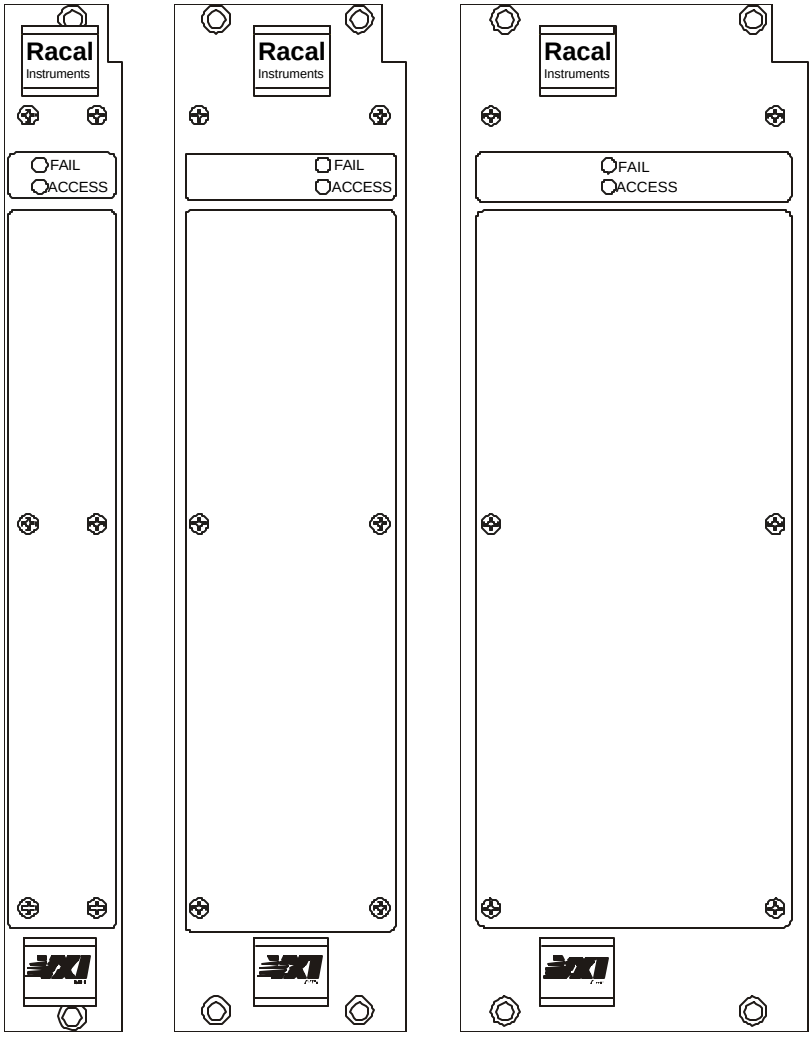
Chapter 1

GENERAL DESCRIPTION

Introduction

This manual contains information on how to install and operate the 7064R in a VXIbus environment. It describes the function and applications of the 7064R Register Based Prototype.



7064R-110 **7064R-210** **7064R-310**

Figure 1-1, 7064R Front Panel

General Description

The 7064R-110,-210,-310 are register based VXIbus development cards that provide the user with access to all 32 bits of the VXIbus backplane (D32).

The 7064R supports 8, 16, and 32-bit Data access and A16, A24 and A32 addressing space.

Eighty square inches of real estate are available to the user, along with all the appropriate VXIbus backplane signals. The development area consists of a universal array with 0.1 inch center holes. Within this array are 77 distributed VCC/GND pads to provide power. All seven VXIbus supply lines are available to the user and are fused, reducing the risk of damage to the backplane. These modules also provide the EMI power filtering required by the VXIbus specifications, removing the need for the user to design this circuitry.

The 7064R is available in single, double or triple slots, (-110,-210,-310) and fits best in applications that are either not complex in nature or that require very high interactive communication speeds. It is also available as a bare board with power supply filtering and fuse protection only as a 7064R-119

These register based VXIbus development cards have been designed to replace the 7064-20 Series of VXI modules. These cards are similar to the 7064-20 with the following major differences:

- The Message Based option interface and the Local Bus interface circuitry was removed to increase the development area.
- Access to the VXIbus TTL Triggers is provided.
- An additional 10 sq.in. in breadboard area.
- ID and Device Type Register Dip switches replaced with jumper pads on the PCB to increase the development area.

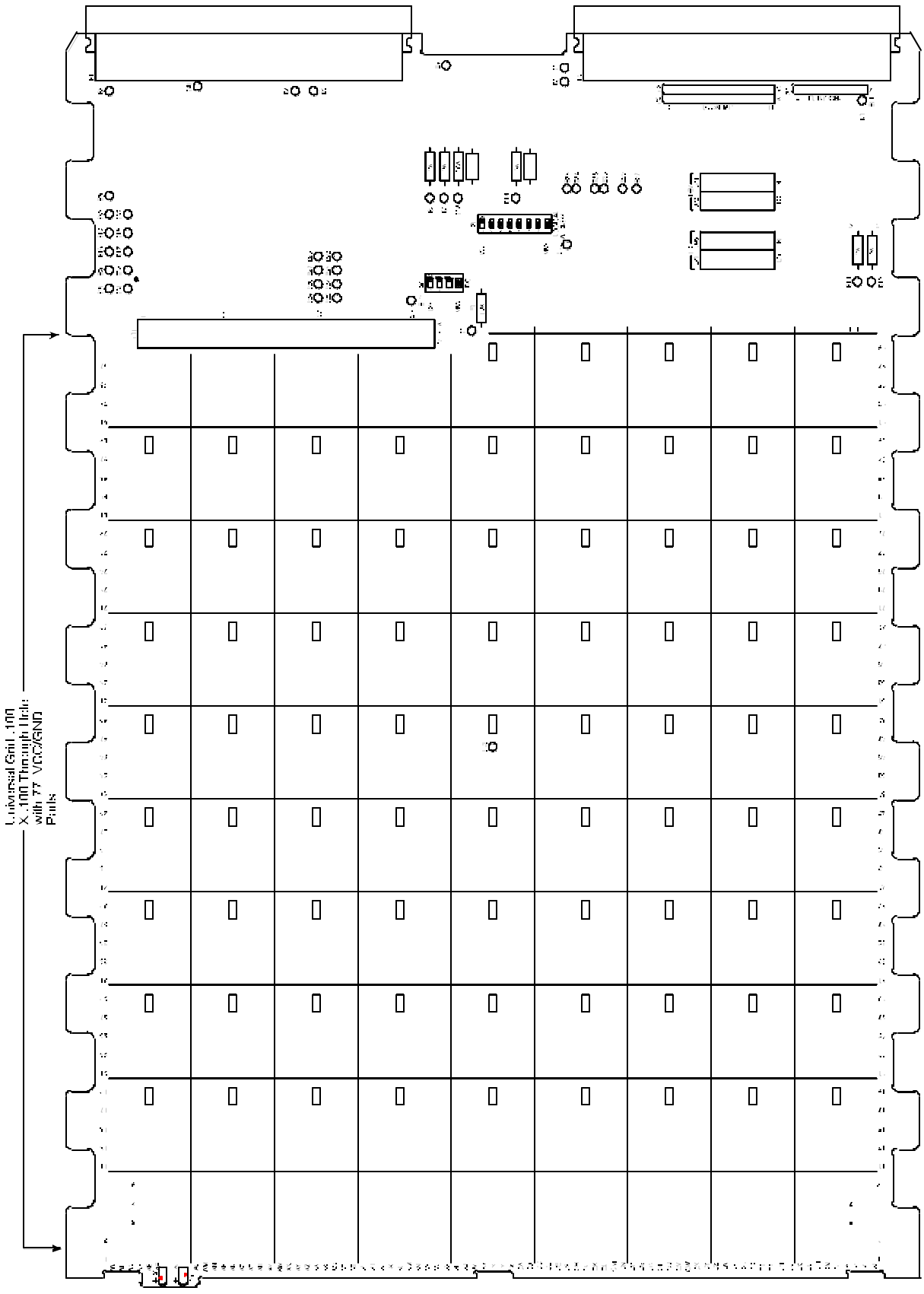


Figure 1-2, 7064R Register-Based Prototype

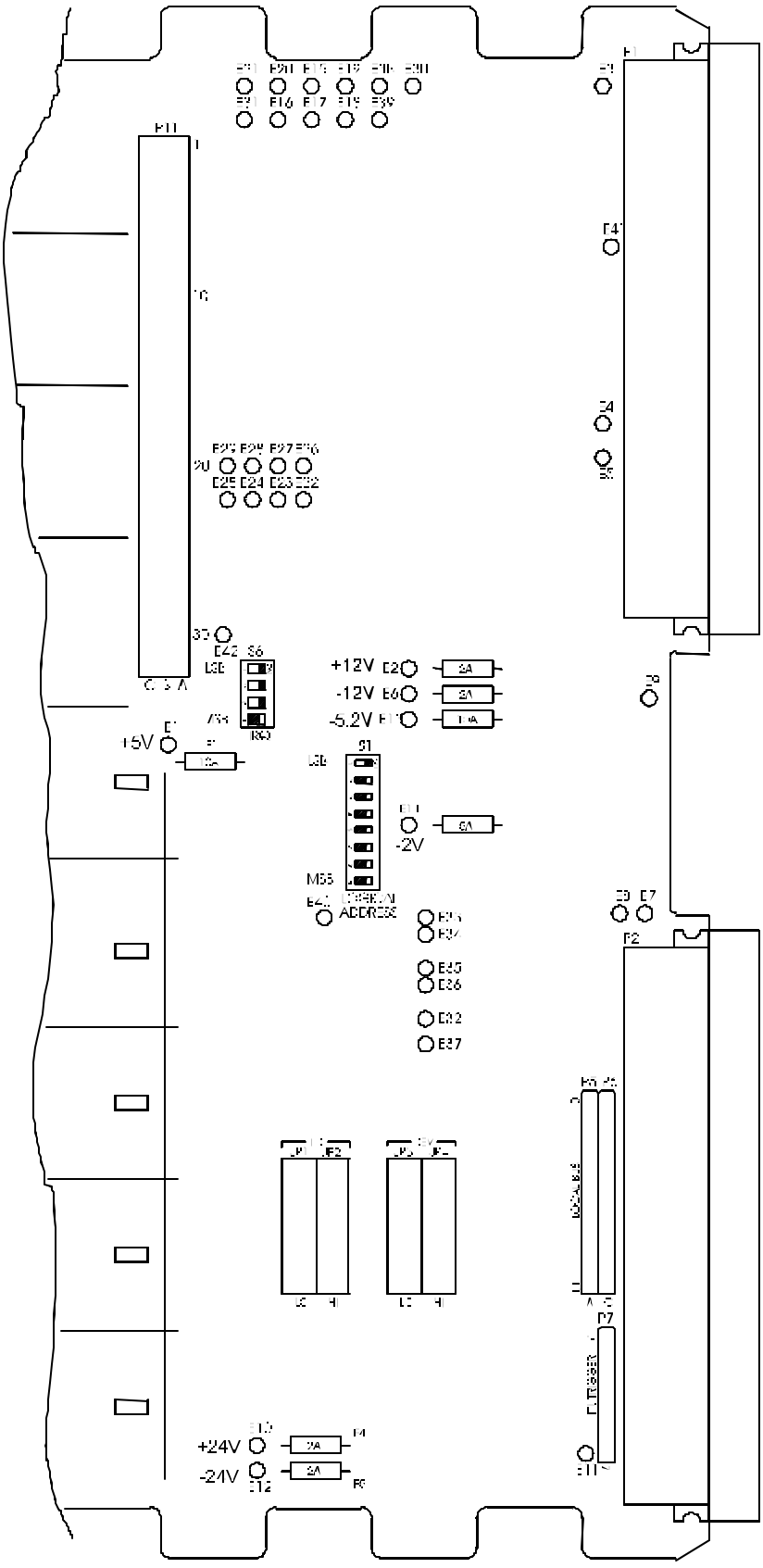


Figure 1-3, Prototype Control and Interface Signals/Power

7064R
Specifications

Table 1-1, Functional Performance

Parameter	Specification
Modes of Operation	VXI Register Based Servant Interrupter
Front panel connectors	None
Front panel controls	None
Front panel indicators	"FAIL" Red LED Indicator "ACCESS" Green LED Indicator
Rear panel connectors [1]	VXI P1/P2 (See VXIbus REV 1.4)
Rear panel controls	None
Rear panel indicators	None
Breadboard Area [1]	80 sq. in.,+5V/Gnd Plane to 77 pads each
Interface Characteristics Manufacturer ID no: Model No: Logical Addressing: Address Space: Data Transfer Bus: Device Class: Interrupt Levels:	VXIbus Interface 4091, Jumper Programmable 4093, Jumper Programmable Static 1-254, Switch Selectable A16 (expandable to A16/A24 or A16/A32) D32, D16, D08(EO) support Register Based Slave Device Programmable 1-7, Switch Selectable

NOTE: 1. This specification also applies to the model 7064R-119. All others do not unless noted.

Table 1-2, 7064R Module Power Requirements

+5 Volts	**Specification**
Peak Current I_{Pm}	750mA
Dynamic Current I_{Pm}	10 mA
-5.2 Volts	**Specification**
Peak Current I_{Pm}	100 mA
Dynamic Current I_{Pm}	1 mA
-2 Volts	**Specification**
Peak Current I_{Pm}	10 mA
Dynamic Current I_{Pm}	1 mA

Table 1-3, Maximum Available User Power

Maximum User Current	Specification
+5V	5 Amps Max.
-5.2V	5 Amps Max.
-2V	2 Amps Max.
+12V	1 Amp Max.
-12V	1 Amp Max.
+24V	1 Amp Max.
-24V	1 Amp Max.

Table 1-4, Cooling Requirements

Parameter	Specification
Maximum Module Power	4.2 Watts (Does not include prototype circuitry)
Minimum Airflow	.35 Liters/sec at .04mm H_2O for a 10^{o}C Rise

Note: Refer to Chapter 3, Module Cooling Considerations

Table 1-5, 7064R Mechanical Parameters

Parameter	Specification		
Enclosure Style	VXI"C" SIZE - Prototype Enclosure		
Enclosure Dimensions (in.)	7064R-110: 14Lx 10.3W x l.2D 7064R-210: 14Lx 10.3W x 2.4D 7064R-310: 14Lx 10.3W x 3.6D		
Module Weight	7064R-110: 1.8 lbs. 7064R-210: 2.1 lbs. 7064R-310: 2.4 lbs.		
Prototype Area Maximum Clearance	**Module**	**Circuit Side**	**Component Side**
	7064R-110	0.13 in.	0.75 in.
	7064R-210	1.30 in.	0.75 in.
	7064R-310	1.30 in.	1.95 in.
User Maintenance Items	No Maintenance Required		

Table 1-6, 7064R Environmental Specifications

Parameter	Specification
Temperature, operating	0^0C to +55^0C
Temperature, non-operating	-40^0C to +71^0C
Relative Humidity	95 +/-5% RH non-condensing;75+/-5 %RH above 30^0C;45+/-5 %RH above 40^0C
Altitude, operating	10,000 ft
Altitude, non-operating	15,000 ft
Vibration	0.013" double amplitude, 5-55Hz
Shock, functional	30g, 11mSec, 1/2 sine wave
Bench handling	4 inch/45^0
Fungus resistance	Yes, fungus inert materials used.

Table 1-7, Reliability and Safety Specifications

Parameter	Specification
MTBF	>500,000 Hours, calculated per MIL-HBK217, ground-benign, 30^0C
MTTR	< 30 minutes
Safety	IEC 1010.1, UL3111-1, CSA 22.2 No. 1010.1
Packaging for shipment	ASTM D4169 Rev. -94

Table 1-8, EMC Specifications

Parameter	Specification
Conducted Emissions	VXIbus Rev 1.4, B.8.7.3
Conducted Susceptibility	VXIbus Rev 1.4, B.8.7.4
Radiated Emissions (Closed Field)	VXIbus Rev 1.4, B.8.6.3
Radiated Susceptibility	VXIbus Rev 1.4, B.8.6.4

DEFINITIONS

EMC	Electro-Magnetic Compatibility
MTBF	Mean Time Between Failure
MTTR	Mean Time To Repair
RH	Relative Humidity

INPUT/OUTPUT Definitions

Unless otherwise specified all logic signals are TTL compatible; "-“, designates an active low signal

Notes:

1. Refer to VXIbus Rev 1.4 for details.

2. Applies to Model 7064R-119 also.

Table 1-9, P1 / P2 Input / Output Descriptions

I/O Signals	Connector	Type	Description
VXIbus Interface	P1/P2		See VXIbus REV 1.4 Specification

Table 1-10, User Interface Connector

I/O Signals	Connector	Type	Description
BA[1-31]	P11-B2 to P11-B32	Out	Buffered VXI Address Bus
BD[0-31]	P11-A1 to P11-A32	In/Out	Buffered VXI Data Bus
BAS-	P11-B1	Out	Buffered VXI Address Strobe
BWRITE-	P11-C30	Out	Buffered VXI Write Control
BLWORD-	P11-C29	Out	Buffered VXI Long Word Control
BDS1-	P11-C28	Out	Buffered VXI Data Strobe
BDS0-	P11-C27	Out	Buffered VXI Data Strobe
BSYSRST-	P11-C26	Out	Buffered VXI System Reset
BSYSCLK	P11-C25	Out	Buffered VXI System Clock
BLOCK-	P11-C24	Out	Decoded "Block" Address Mode
PROG/DATA-	P11-C23	Out	Decoded "Data" Address Mode
A32ENA-	P11-C22	Out	Extended Address Mode Decode
A24ENA-	P11-C21	Out	Standard Address Mode Decode
A16ENA-	P11-C20	Out	Short Address Mode Decode
MYVXIENA-	P11-C19	Out	Local VXI Address Decode
VXIENA-	P11-C18	Out	VXI Address Space Decode
WRTBASE+E-	P11-C16	Out	Register Write Control –“E”
WRTBASE+C-	P11-C15	Out	Register Write Control - "C"
WRTBASE+A-	P11-C14	Out	Register Write Control - "A"
WRTBASE+8-	P11-C13	Out	Register Write Control - "8"
WRTBASE+6-	P11-C12	Out	Register Write Control - "6"
WRTBASE+2-	P11-C11	Out	Register Write Control - "2"
WRTBASE+0-	P11-C10	Out	Register Write Control - "0"

RDBASE+E-	P11-C8	Out	Register Read Control - "E"
RDBASE+C-	P11-C7	Out	Register Read Control - "C"
RDBASE+A-	P11-C6	Out	Register Read Control - "A"
RDBASE+8-	P11-CS	Out	Register Read Control - "8"
RDBASE+6-	P11-C4	Out	Register Read Control - "6"
USEREN-	P11-C2	In	User Address Decode Enable
USRDTACK-	P11-C3	In	User Data Transfer Acknowledge.
IRQIN-	P11-C31	In	User Interrupt Request
CLRIRQ-	P11-C32	In	User Interrupt Clear
GND [2]	P11-C1 P11-C9 P11-C17	Pwr	Signal Ground

Table 1-11, P5 / P6 / P7 Input / Output Descriptions

I/O Signals	Connector	Type	Description
LOCAL BUS A [0-11] [2]	P5-1 to P5-12	In / Out	VXIbus Local Bus A [1]
LOCAL BUS C [0-11] [2]	P6-1 to P6-12	In / Out	VXIbus Local Bus C [1]
TTLTRG[0-7]- [2]	P7-1 to P7-8	In / Out	VXIbus TTL Trigger [1]

Table 1-12, User "E" Point Input / Output Descriptions

I/O Signals	E Point	Type	Description
+5V [2]	E1	Pwr	Filtered,10A fused,+5 Volts
+12v [2]	E2	Pwr	Filtered,2A fused,+12 Volts
ACFAIL- [2]	E3	Out	AC Power Fail [1]
SERCLK- [2]	E4	Out	Serial Clock [1]
SERDAT- [2]	E5	In / Out	Serial Data [1]
-12V [2]	E6	Pwr	Filtered,2A fused,-12 Volts
CLK1O+ [2]	E7	Out	10 Mhz Diff. Clock [1]
CLK1O- [2]	E8	Out	10 Mhz Diff. Clock [1]
+5VSTDBY [2]	E9	Pwr	+5Volt Standby [1]
+24V [2]	E10	Pwr	Filtered,2A fused,+24 Volts
SUMBUS [2]	E11	In / Out	Current Sum Bus [1]
-24V [2]	E12	Pwr	Filtered,2A fused,-24 Volts
-5.2V [2]	E13	Pwr	Filtered,5A fused,-5.2 Volts
-2V [2]	E14	Pwr	Filtered,2A fused,-2 Volts
STATREGEN-	E15	Out	Status Register Read Enable
PASSED	E16	In	Passed Status Bit 2 [1]
READY	E17	In	Ready Status Bit 3 [1]
DEVSTAT0	E18	In	Device Status Bit 0 [1]

DEVSTAT1	E19	In	Device Status Bit 1 [1]
DEVSTAT4	E20	In	Device Status Bit 4 [1]
DEVSTAT5	E21	In	Device Status Bit 5 [1]
CTRLREGEN-	E22	Out	Control Register Write
SRESET	E23	Out	Soft Reset Bit 0 [1]
SYSFAILINH	E24	Out	System Fail Inhibit Bit 1 [1]
DEVCTRL2	E25	Out	Device Control Bit 2 [1]
DEVCTRL3	E26	Out	Device Control Bit 3 [1]
DEVCTRL4	E27	Out	Device Control Bit 4 [1]
DEVCTRL5	E28	Out	Device Control Bit 5 [1]
DEVCTRL6	E29	Out	Device Control Bit 6 [1]
A24/A32EN	E30	Out	A24/A32 Address Enable Bit 15 [1]
USRSYSFAIL-	E31	In	User Buffered System Fail
ECLTRG0-	E32	In	ECL Buffered Trigger 0
ECLTRGIN0-	E33	Out	Differential ECL Trigger 0-
ECLTRGIN0	E34	Out	Differential ECL Trigger 0
ECLTRGIN1-	E35	Out	Differential ECL Trigger 1-
ECLTRGIN1	E36	Out	Differential ECL Trigger 1
ECLTRG1-	E37	In	ECL Buffered Trigger 1
MYDTACKIN-	E38	In	Data Transfer Ack. Input
MYDTACKOUT-	E39	Out	Data Transfer Ack. Output
IRQEN-	E40	Out	Interrupt Status Read Enable
BERR- [2]	E41	Out	Bus Error [1]
INSTRST-	E42	Out	Instrument Reset
CHASSIS	E43	--	Chassis Ground
RDEN-	E44	Out	VXI A16 Read Strobe
WREN-	E45	Out	VXI A16 Write Strobe

Options

Model / Option	Part No.	Description
7064R-110	407620-110	Single Slot Register Based Proto, Module
7064R-210	407620-210	Double Slot Register Based Proto, Module
7064R-310	407620-310	Triple Slot Register Based Proto, Module
7064R-119	407620-119	Prototype, Bare Board
7064R-001	407620-001	Single-slot Prototyping Module, Enclosure only
7064R-002	407620-002	Double-slot Prototyping Module, Enclosure only
7064R-003	407620-003	Triple-slot Prototyping Module, Enclosure only
980817	980817	7064R – Additional Instruction Manual

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Chapter 2

INSTALLATION INSTRUCTIONS

Introduction

This section describes the unpacking, inspection, set-up and installation of the Model 7064R Register Based Prototype module in a C-size mainframe.

Unpacking and Inspection

1. Before unpacking the 7064R module, check the exterior of the shipping carton for any damage. If the shipping carton is damaged, inform the carrier immediately.

2. Remove the 7064R module and inspect it for damage. If any damage is apparent, inform the carrier immediately. Retain shipping carton and packing material for the carrier's inspection.

3. Verify that the pieces in the package you received contain the correct 7064R module option and the 7064R Users Manual. Notify Racal Instruments if the module appears damaged in any way. Do not attempt to install a damaged module into a VXI chassis.

4. The 7064R module is shipped in an anti-static bag to prevent electrostatic damage to the module. Do not remove the module from the anti-static bag unless it is in a static-controlled area.

Address Switch Settings for Configuration Control

The 7064R Register Based Prototype Module has an internal 8-position address dip switch, S1, used to determine the static configuration. It is located on the top of the module, accessible through the case.

In the ON position, the switch is set to logical 1, and in the OFF position to a logical 0.

The user can select any logical address from 1 to 254 for static configuration.

NOTE

Logical address 0 is not allowed. Logical address 255 is not allowed because it is used for modules that support dynamic configuration.

NOTE

The 7064R Register Based Breadboard Module is shipped with the logical address set for 1. Refer to the Resource Manager's manual for details about addressing methods.

VXIbus Interrupt Level Switch Settings

The 7064R Register Based Prototype has an internal 4-position interrupt level dip switch, S6, used to set the module priority interrupt level. It is located on top of the module and can be accessed by first removing the top cover screws and sliding out the module enclosure top cover. The default setting is Interrupt Level 7.

In the ON position, the switch is set to logical 1, and in the OFF position to a logical 0. The user can select any interrupt level from 1 to 7 by setting switch positions 1-3 (switch position 4 is not used).

7064R to VXIbus Main Frame Installation

The 7064R Register Based module is ready for operation when shipped. The address switch is set to 1. The interrupt level switch is set for level 7.

To install the 7064R in a C-size VXI chassis, use the following instructions:

1. Ensure power is OFF.

2. Configure the interrupt daisy chain on the backplane to bypass empty slots, per VXIbus specifications.

3. Remove the front cover of the VXI chassis, and slide the 7064R into the appropriate slot with the LED’s towards the top (or to the left when using a horizontal chassis).

NOTE:

There is no need to configure the VXI Backplane Slot used for the 7064R Register Based Prototype, since all BUSGRANT and IACK signal lines are passed to the next slot.

Power-up Initialization

Before turning on the VXIbus mainframe, make sure a Slot 0 with a Resource Manager is present. Upon power-up of the system, the 7064R goes through the following power-up sequence:

- The 7064R Register Based Prototype module has two LED's on the front panel – FAIL and ACCESS. The LED functions are:

  FAIL• On during a (user provided) self-test
  Off when the (user provided) self-test has successfully completed

  ACCESS• Blinks on when the VXIbus is accessing the 7064R Module

Local Bus Usage with 7064R Register Based Prototype

The VXIbus has a provision for interconnecting adjacent cards through a local bus. The VXIbus backplane consists of 12 lines which jumper cards together. A card on the left of another will have connections on the "C" side of P2 tied to the "A" side of P2 for the card to its right. The 12 lines can then be connected through the 7064R module and form a bus connection to a group of modules within a VXI chassis. (Refer to the VXIbus specification for exact pinouts.)

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Chapter 3

REGISTER-BASED PROTOTYPE APPLICATIONS

INTRODUCTION

The 7064R Register Based Prototype Module has many features and great flexibility. This information describes some of the features, and gives examples of how typical circuits can be implemented.

VXI REGISTERS

All VXIbus devices have a set of registers that appears in the A16 address space. Each device is given 64 bytes of A16 address space for its registers. Register-based devices have four 16-bit registers that are normally implemented. Three of these registers are read registers. They are ID Register, Device Type Register, and Status Register. There is one Write Register - the Control Register. There is an optional Read/Write Register called the Offset Register. The remaining A16 address space beyond the lower four registers is devoted to device dependent registers. These registers can be used for any desired purpose.

Status Register

There are 12 bits in the Status Register that are device dependent. They can be used by the instrument designer for whatever purpose is desired. The Register Based Prototype implements four of these device dependent bits. These bits are controlled by the levels at E18, E19, E20 and E21. The designer can also control the PASSED and READY bits in the Status Register by controlling the levels of E16 and E17. The MODID bit is automatically controlled by the MODID bit on the backplane. The A24/A32 bit is automatically controlled by the A24/A32 enable bit in the control register. If the device designer wants to implement the additional device dependent bits (6 through 13), that is easily accomplished with one additional IC. Here is an example circuit that shows how it can be done:

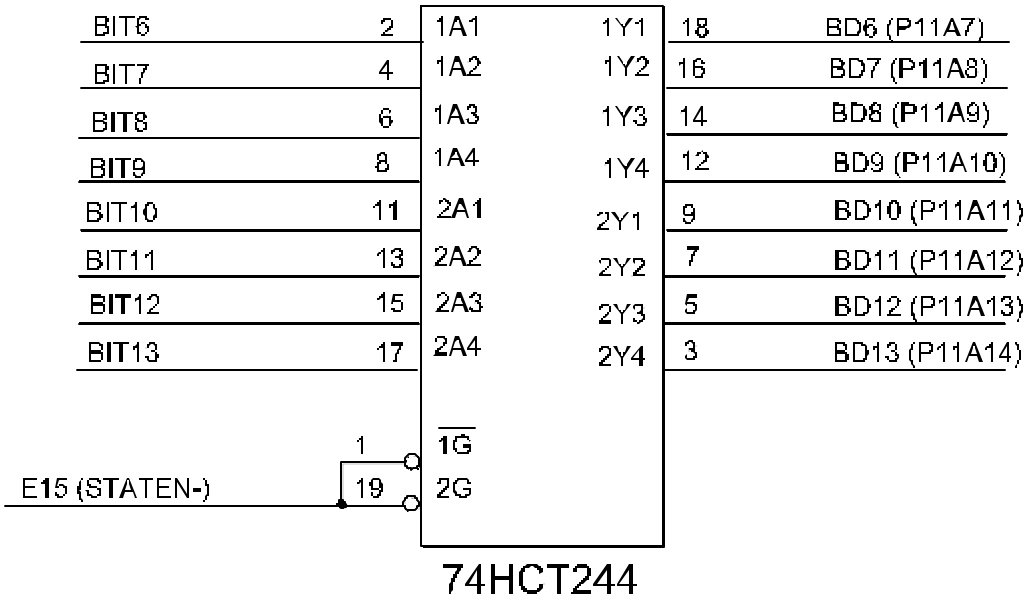


Figure 3-1, VXI Status Register Expansion

Control Register

The Control Register is reset at power-up by a buffered version of the SYSRESET signal from the backplane (BSYSRST-). The prototype also provides the reset bit SRESET out of the Control Register at E23. This can be used to drive other circuitry that is dependent on this bit.

NOTE

SRESET is not the same as the SYSRESET bit from the backplane. It is a bit the system controller uses to force a device into a reset state (the BSYSRST- signal is provided at P11-C26).

An additional reset signal, INSTRST- E42, is provided which is reset by either SYSRST- being low or the Control Register reset bit 0 being high.

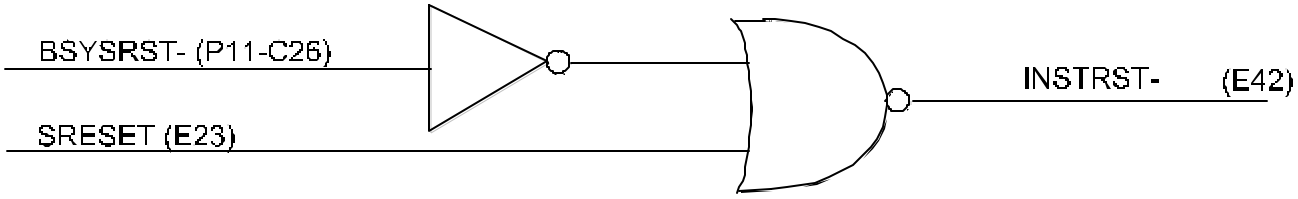


Figure 3-2, Instrument Reset

Another bit in the Control Register is SYSFAIL INHIBIT. This bit is found at E24. The SYSFAIL INHIBIT is used by the system controller to disable the SYSFAIL line on the backplane even though the local board might have a fail condition. Normally the user will drive E31 low to indicate that any Power Up Self-Test has failed. This signal, USRSYSFAIL-, defaults to the inactive state if not used. The most significant bit defined in the Control Register is A24/A32ENA. This bit is available at E30. This is generally used to tell a device whether extended addressing beyond A16 is available. This bit would be used if A24 or A32 VXI memory were to be put on the instrument. The prototype also has five device dependent bits available (bits 2 through 6) from the Control Register which appear at E25 through E29. The instrument designer can use these bits for whatever purpose is desired. Writes to the Control Register affect these bits. If more bits are desired, the designer can use a single chip to implement the rest of the device dependent bits of the Control Register as shown in figure 3-3:

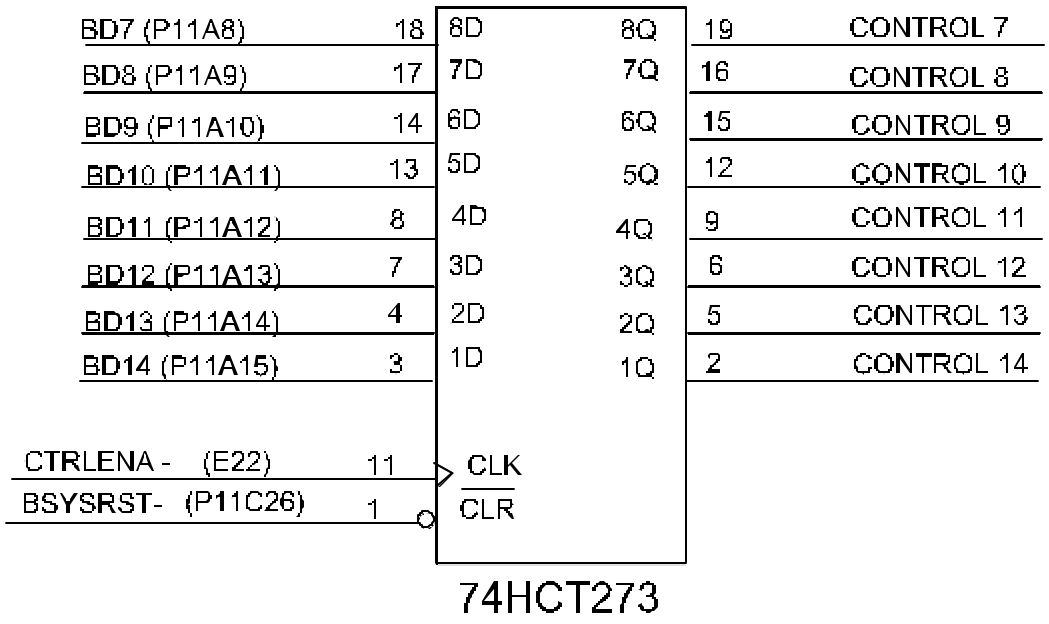


Figure 3-3, VXI Control Register Expansion

ID Register

The 7064R Prototype module implements all bits of the ID Register. The bits are controlled by Jumpers JP1 and JP2. The jumpers and the bits they control are shown on page 3-19. These bits are used to identify the manufacturer, the address space and the device class. Manufacturer ID numbers are obtained from the VXIbus consortium. Address space indicates the addressing modes of the device's operational registers (e.g., A16 only is indicated by both bits set high). Device class refers to the type of instrument (e.g., register-based is indicated by both bits set high). Refer to page 3-19 for detailed information.

Device Type Register

The 7064R Prototype module implements all bits of the Device Type Register. The bits are controlled by Jumpers JP3 and JP4. The jumpers and the bits they control are shown on page 3-20. These bits are used to identify the instrument model and tell how much memory space is required by this instrument. The manufacturer is at liberty to set the model to almost any code desired.

NOTE

Model codes 0 and 255 are reserved for slot 0 devices, and in most cases, should not be used.

Required memory is indicated by the upper four bits of the device type register. If the instrument is an A16 only device, the upper four bits are used as an extension of the model number. Refer to page 3-20 for detailed information.

Additional VXI Read Registers Using Internal Decoding

The 7064R provides decoding for five additional read registers. Because each decoded control signal is for 16 bits and the internal bus is 32 bits wide, **the user must pay careful attention to which group of 16 data bits is used**. Controls RBASE+8 and RBASE+C should be used with BD0 through BD15. Controls RBASE+6, RBASE+A and RBASE+E should be used with BD16 through BD31. Controller accesses of 16 and 32 bits are automatically handled. The decoded control signals appear at P11, the user interface connector. An example of how some registers can be added is shown in Figure 3-4.

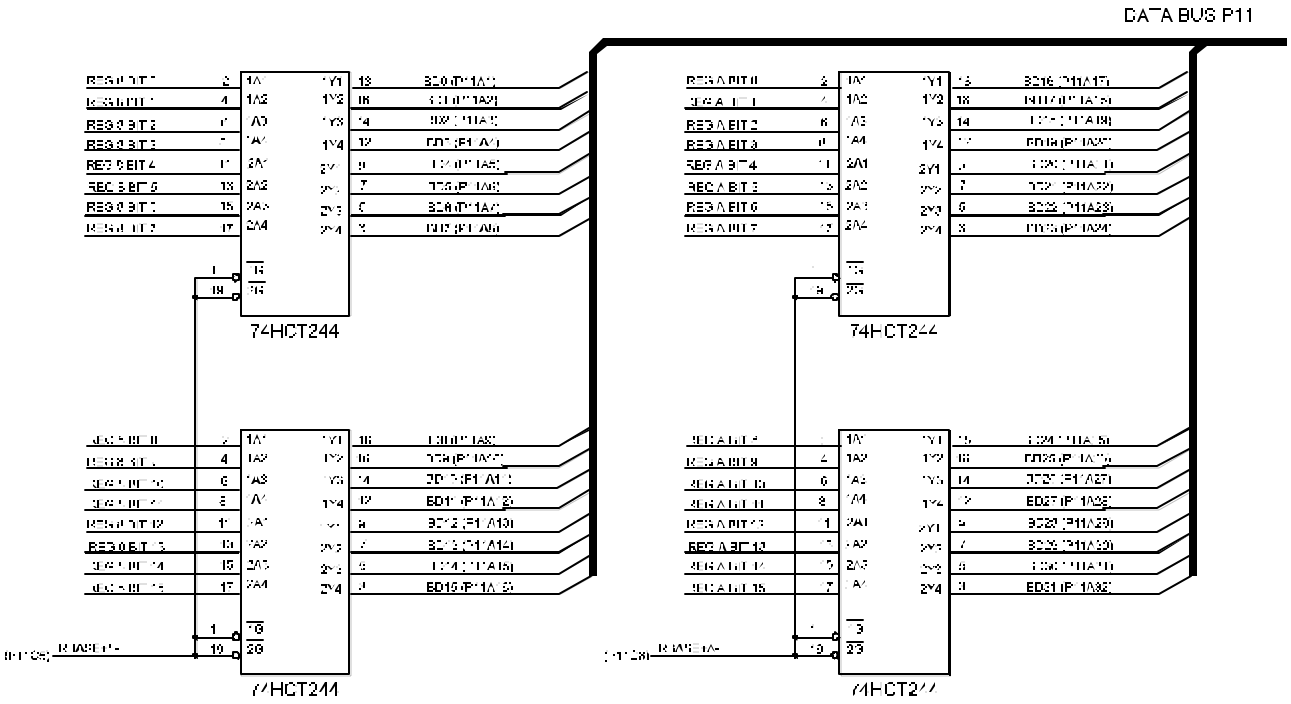


Figure 3-4, Additional Read Registers Using Internal Decoding

When using the INTERNAL Read decoding of the 7064R, the maximum access time of the device register must be less than 150nSec. If the user needs to extend the required access time for a device, a method for doing this is shown in Figure 3-5.

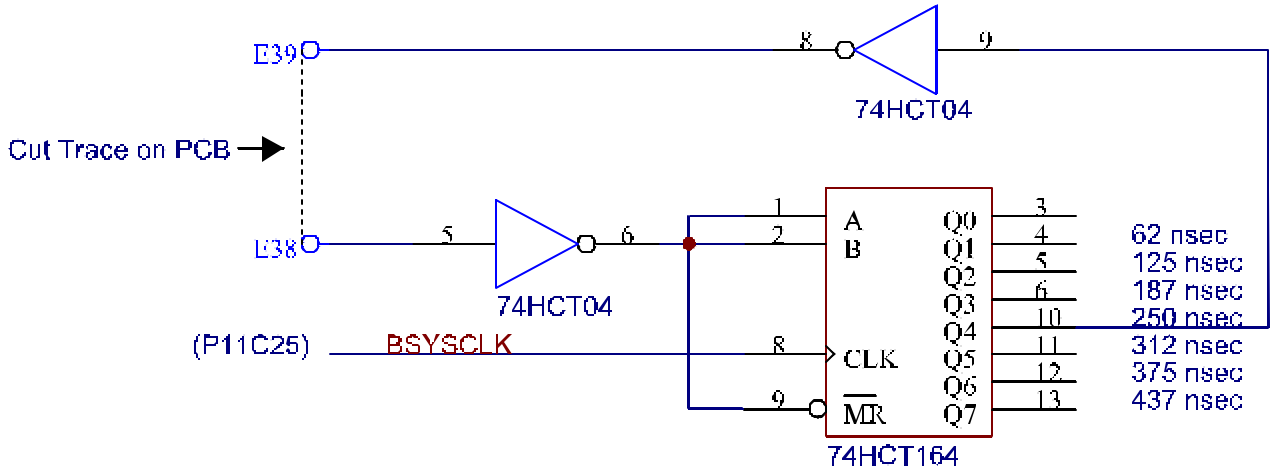


Figure 3-5, DTACK Delay Generator

Additional VXI Write Registers Using Internal Decoding

The 7064R provides decoding for seven additional write registers. Because each decoded control signal is for 16 bits and the internal bus is 32 bits wide, **the user must pay careful attention to which group of 16 data bits is used**. Controls WBASE+0,WBASE+8, and WBASE+C should be used with BD0 through BD15. Controls WBASE+2,WBASE+6, WBASE+A and WBASE+E should be used with BD16 through BD31. When using the INTERNAL Write decoding of the 7064R, the typical data setup time of the device register is 300nSec and the typical hold time is at least 50nSec. If a device register setup time needs to be extended, a method for doing so is shown in Figure 3-5. Controller accesses of 16 and 32 bits are automatically handled. The decoded control signals appear at P11, the user interface connector. Here is an example of how some additional registers can be added.

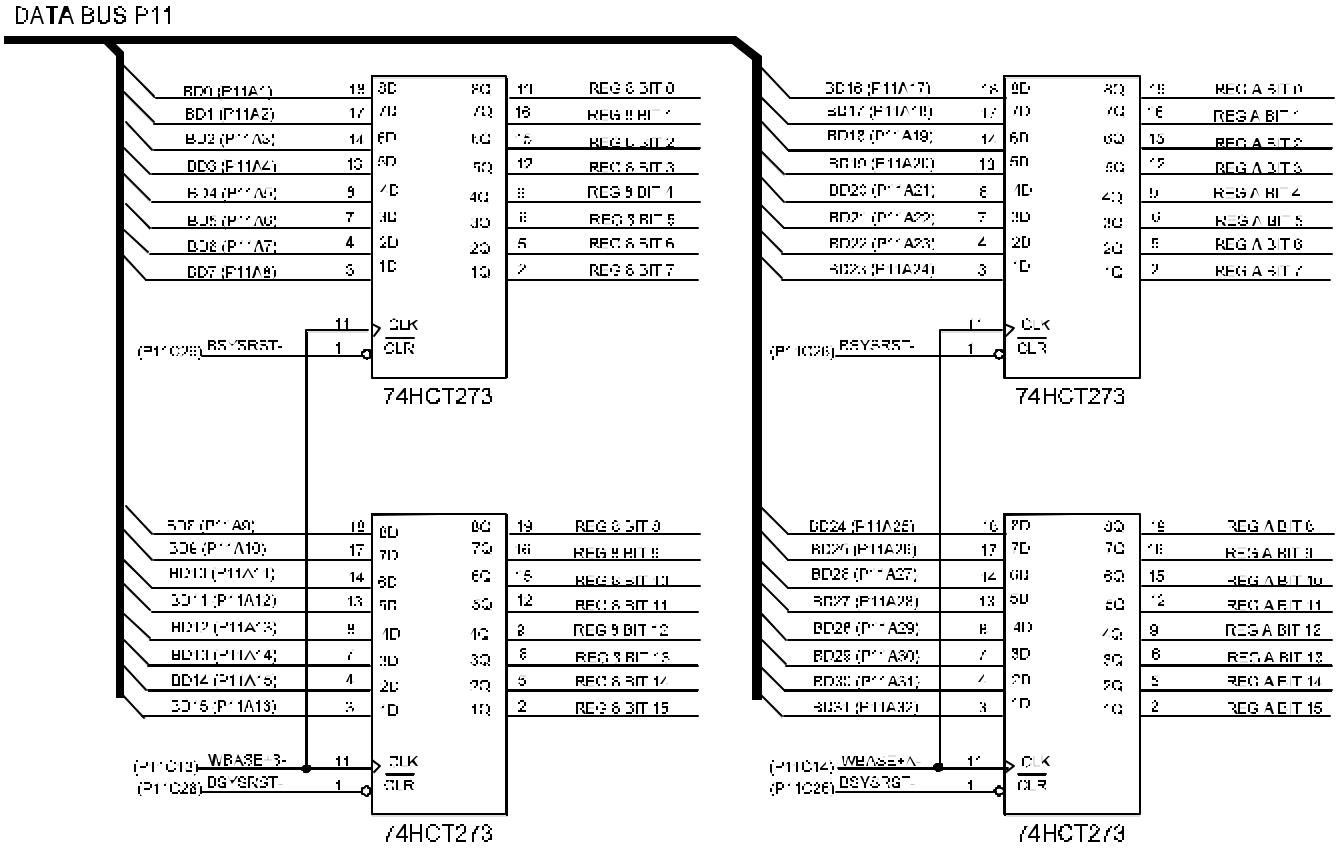
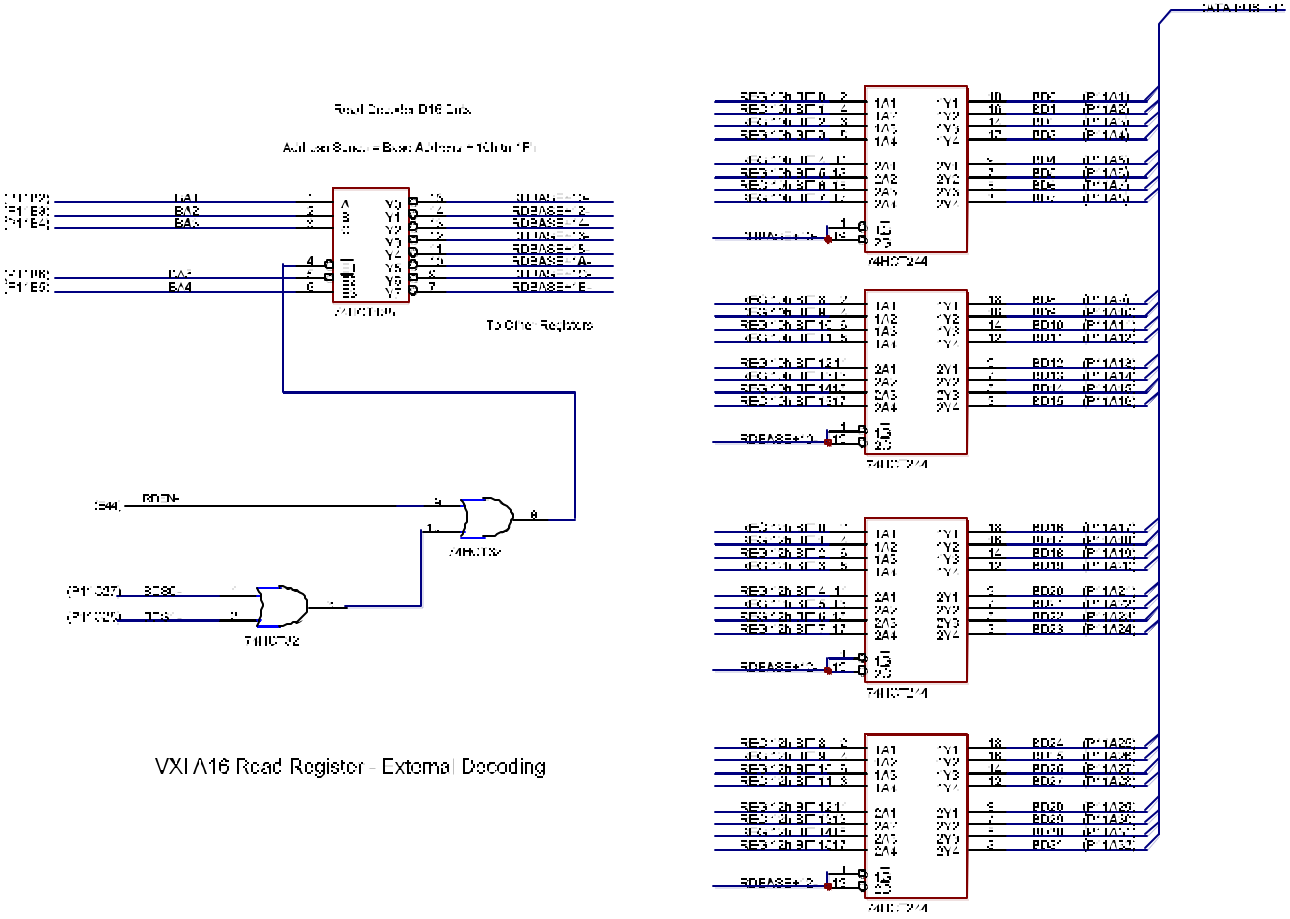


Figure 3-6, VXI A16 Write Registers Using Internal Decoding

Additional VXI Read Registers Using External Decoding

If additional Read registers are required for expanding the prototype device register space, (addresses 10h to 3Fh), external decoding circuitry is required. Since the internal Databus is 32 bits wide, the user must also **pay careful attention to which group of 16 data bits is used**. The signals that need to be decoded for additional registers are available at P11, the user interface connector. Here is an example of an external decoder circuit for additional read registers. If the bus transfer cycle time needs to be lengthened use the DTACK delay generator circuit in Figure 3-5



VXI A16 Read Register - External Decoding

Figure 3-7, VXI A16 Read Register Using External Decoding

Additional VXI Write Registers Using External Decoding

If additional Write registers are required for expanding the prototype device register space, (address 10h to 3Fh), external decoding circuitry is required. Since the internal Databus is 32 bits wide, the user must also **pay careful attention to which group of 16 data bits is used**. The signals that need to be decoded for additional registers are available at P11, the user interface connector. Here is an example of an external decoder for additional write registers. If the bus transfer cycle time needs to be lengthened use the DTACK delay generator circuit in Figure 3-5

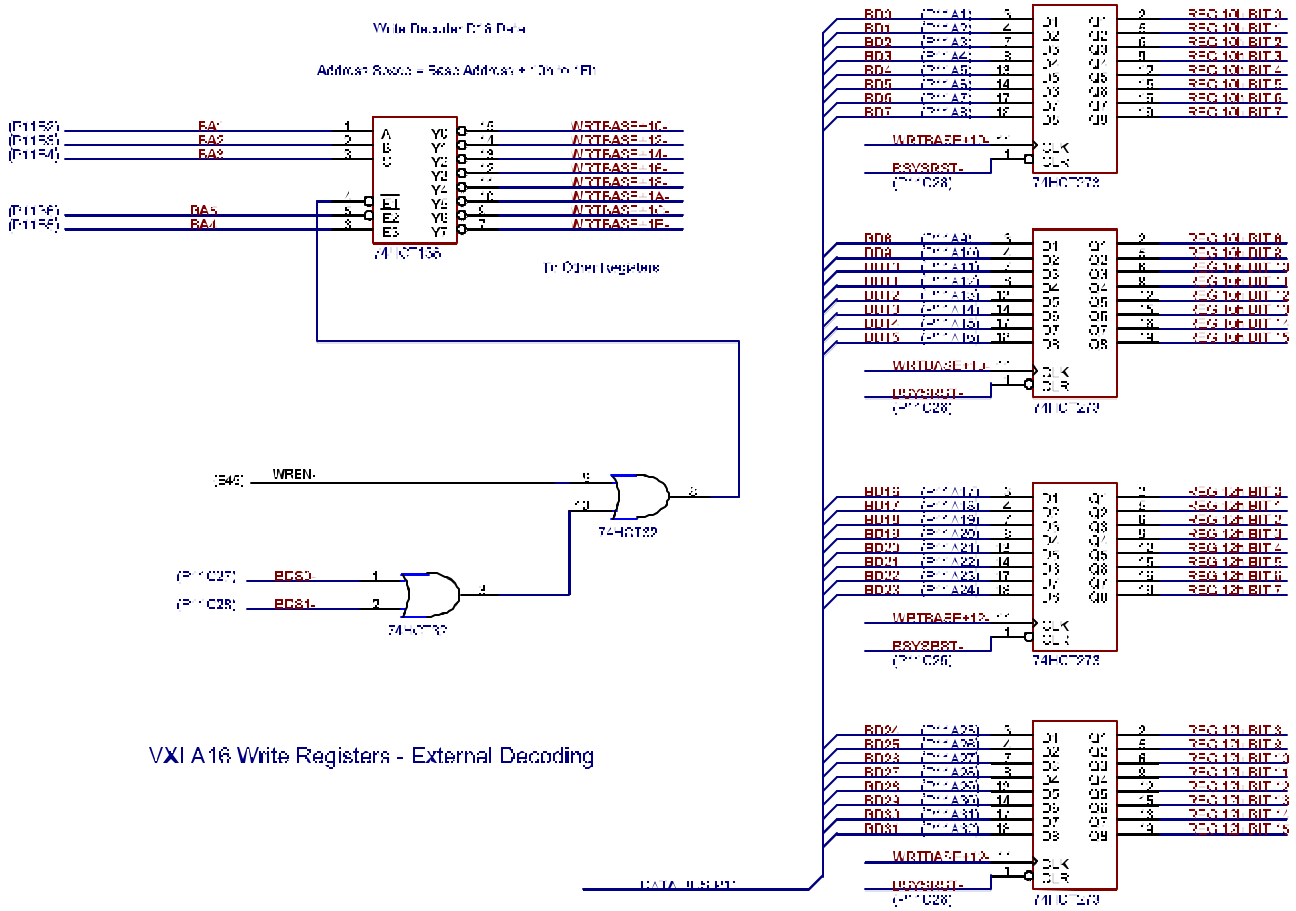


Figure 3-8, VXI A16 Write Registers Using External Decoding

A24/A32 Addressing

The user may further expand the prototype address space by using A24 or A32 addressing modes. This is typically used for memory type devices or where the VXI A16 Address space can not handle the number of registers on the module (64 bytes per module max.). Details of A24/A32 addressing modes can be found in VXIbus Specifications Revision 1.4, sections C.2.1.1.2 and C.2.1.1.5. An example of a typical circuit required to interface to A24 address space is shown in Figure 3-9. Note that the user A24 address decoder output is sent to the 7064R internal circuitry via USREN- to start a bus transfer cycle. Also note that the user must provide a local DTACK signal USRDTACK- to complete the data transfer cycle. All DTACK timing is the responsibility of the user.

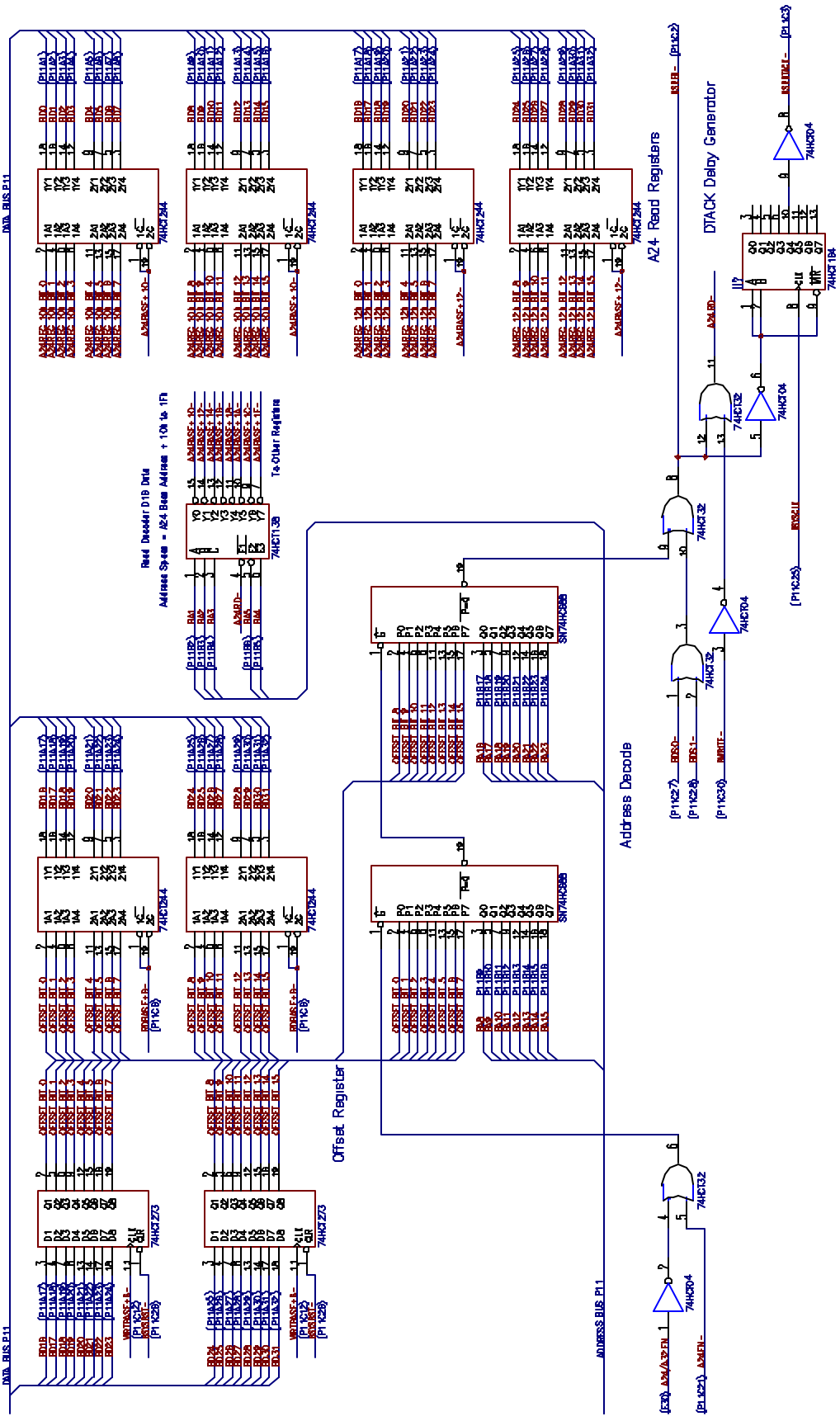


Figure 3-9, VXI A24 Read Register Using External Decoding

The 7064R provides decoded Address modifier outputs that can be used for Address decoding. These signals are available at the P11 connector as follows:

Table 3-1, Signals Available at P11

SIGNAL	LOCATION
VXIEN-	P11-C18
MYVXIEN-	P11-C19
A16EN-	P11-C20
A24EN-	P11-C21
A32EN-	P11-C22
PROG/DATA-	P11-C23
BLOCK-	P11-C24

Interrupt Control

The 7064R Register Based Prototype module has the ability to generate prioritized VXI interrupts to the Slot 0 Resource Manager. A typical interrupt sequence would be as follows. The user would start the sequence by driving the signal line IRQIN-(P11-C31) low. This is an edge sensitive interrupt input. The 7064R would subsequently drive the S6 switch selected interrupt level on the VXI backplane. The VXI interrupt handler will initiate the level specific interrupt acknowledge cycle. The 7064R will respond by returning its STATUS/ID word to the handler to identify that it is the source of the interrupt. Normally the interrupt request is released on the interrupt acknowledge cycle (ROAK). The user can disable any interrupt from occuring by driving the IRQCLR-(P11-C32) line low. The user can expand the STATUS/ID Register and use the device dependent Cause/Status field of the register. An example of a circuit that shows how this can be done is shown in the following diagram.

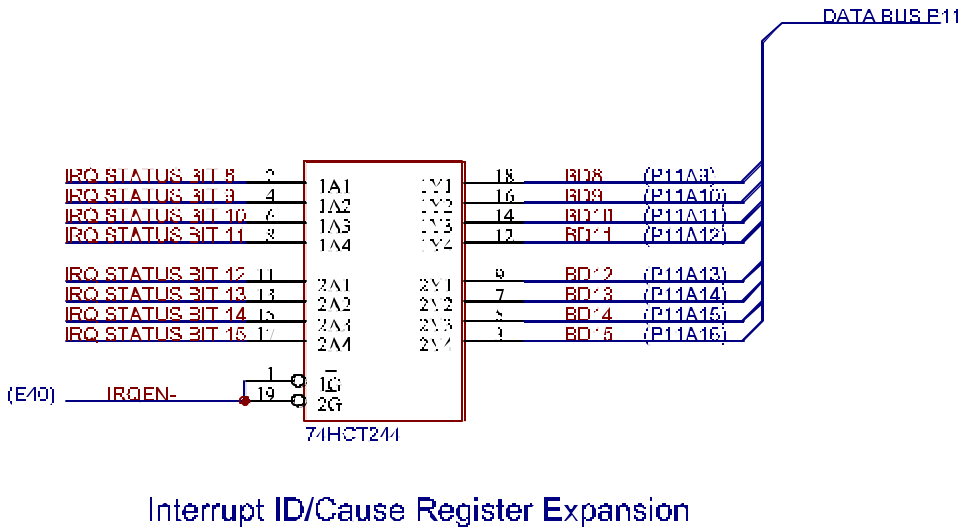


Figure 3-10, Interrupt ID/Cause Register Expansion

Prototype Voltages

The 7064R Register Based Prototype module provides filtered and fused VXI supply voltages on the board. The user can access these voltages for his prototyping circuitry. The VXI voltages available are:

Table 3-2, Prototype Voltages

Voltage	Max Current	Fuse	E-Point
+5V	5Amps Max	10A	E1
+12V	1Amp Max	2A	E2
+24V	1Amp Max	2A	E10
- 5.2V	5Amp Max	10A	E13
- 2V	2Amp Max	5A	E14
- 12V	1Amp Max	2A	E6
- 24V	1Amp Max	2A	E12

Note: All fuses are Littlefuse 255 Series or equivalent.

+5V and Ground are distributed throughout the prototype area. There are 77 +5V/Ground power pads throughout the prototype area. A connection to the VXI Chassis is provided at Point E43 of the 7064R Register Based Prototype Module.

Local Bus

Direct access to the VXI Local Bus is provided on the 7064R Register Based Prototype Module. The VXI Local Bus allows communication between modules in adjacent slots of a VXI chassis. Local Bus “A” is connected to the module on the left. Local Bus “C” is connected to the module to the right. The user should exercise caution when using the Local Bus to insure module-to-module compatibility. Refer to VXI Rev. 1.4 Section B6.2.6 and B7.3.7 for further explanation of the VXI Local Bus. Connections are provided as follows on the 7064R:

P5 pin 1	Local Bus A0
P5 pin 2	Local Bus A1
P5 pin 3	Local Bus A2
P5 pin 4	Local Bus A3
P5 pin 5	Local Bus A4
P5 pin 6	Local Bus A5
P5 pin 7	Local Bus A6
P5 pin 8	Local Bus A7
P5 pin 9	Local Bus A8
P5 pin 10	Local Bus A9
P5 pin 11	Local Bus A10
P5 pin 12	Local Bus A11

P6 pin 1	Local Bus C0
P6 pin 2	Local Bus C1
P6 pin 3	Local Bus C2
P6 pin 4	Local Bus C3
P6 pin 5	Local Bus C4
P6 pin 6	Local Bus C5
P6 pin 7	Local Bus C6
P6 pin 8	Local Bus C7
P6 pin 9	Local Bus C8
P6 pin 10	Local Bus C9
P6 pin 11	Local Bus C10
P6 pin 12	Local Bus C11

ECL Triggers

The 7064R provides access to the VXI ECL Trigger Lines. These lines are buffered on the 7064R to minimize stub length, as well as provide high current drive capability required per the VXI specification. Typically these lines are used for synchronization of timing between modules within the VXI chassis. The driver and receiver circuitry are separate on the 7064R Register Based Module.

The ECL driver circuitry provides an inverted buffer (10H123) that has 25 ohm drive capability. The input to the buffer is a 100 ohm impedance that is normally biased to -0.8VDC (ECL logic 1) in order to disable the drivers on the VXI ECL trigger bus. The user

can connect to the buffers at E32 (ECLTRG0) or E37 (ECLTRG1).

The receiver (10H116) on the 7064R outputs a buffered ECL differential signal from the VXI ECL Trigger lines. These differential outputs are open emitter and must be resistor terminated to the -2V(E14) or the -5.2V(E13) supplies. The user can connect to these lines as shown:

ECLTRGIN0	E34
ECLTRGIN0-	E33
ECLTRGIN1	E36
ECLTRGIN1-	E35

TTL Trigger Lines

The 7064R Register Based Prototype Module provides direct access to the VXI TTL Trigger lines. These lines are typically used for intermodule communication applications such as trigger, hand shake, clock, or logic state transmission. They are open collector active low signals and pulled high (inactive) by the VXI backplane. Several standard communication protocols are defined by VXI Rev. 1.4 Refer to section B6.2.3 of the VXI Rev. 1.4 specification for further details. The TTL Trigger connections are defined below:

P7 pin 1	TTLTRG0-
P7 pin 2	TTLTRG1-
P7 pin 3	TTLTRG2-
P7 pin 4	TTLTRG3-
P7 pin 5	TTLTRG4-
P7 pin 6	TTLTRG5-
P7 pin 7	TTLTRG6-
P7 pin 8	TTLTRG7-

Miscellaneous VXI Signals

The 7064R provides direct access to various VXI defined signals. Details of each of these signals can be found in the VXI Rev. 1.4 specifications. Connections to these signals are as follows.

Signal Name	**E-Point**
ACFAIL-	E3
SERCLK	E4
SERDAT-	E5
CLK10-	E7
CLK10-	E8
SUMBUS	E11
BERR-	E41
+5VSTDBY	E9

Module Cooling Considerations

VXI modules are specified to require a particular airflow to maintain a specific temperature rise, which is typically 10° Celsius. The airflow and back-pressure (pressure change across the module) values determine a single operating point that may be plotted on a VXI mainframe cooling curve. If the operating point lies under the mainframe cooling curve, there is a high probability that the module will remain within its specified temperature rise. If the operating point is above the mainframe cooling curve, the temperature rise of the module may exceed the specified value.

Calculated Module Operating Point

A calculation of the operating point or cooling requirements for the 7064R (and user circuitry) can be determined if the total power dissipation is known. This is detailed below.

CAUTION

A module with hot spots or airflow restrictions may require increased airflow. Refer to the VXIbus Specification Revision 1.4 for details.

To calculate the module operating point:

1. Determine the desired maximum temperature rise allowed across the module. This is typically 10°C, but may be higher or lower depending on the specified operating environment, function of the module, part sensitivities, etc.

2. Determine the maximum power in watts dissipated inside the module ($4.2W + P_{user\ circuitry}$).

3. Determine the airflow required by the module to maintain the desired temperature rise. In most cases, this is calculated from the power, desired temperature rise, and the specific heat of air. (For a 10°C rise, airflow in liters/sec=0.08 * power in watts.) The required airflow may be increased or decreased depending on hot spots, airflow blockages, etc.

4. Determine the pressure drop across the module when the specified airflow (in liters/sec) is forced through the module. A reasonable estimate may be calculated from the equation for a typically dense VXI module: $P=0.02G^2 + 0.05G$. (P is pressure in mmH_2O and G is airflow in liters per second.)

5. Plot the module operating point [Pressure (mm of H_2O), Airflow (liters/sec)] on the mainframe curve. If the module operating point lies under the mainframe cooling curve, the module should remain within its specified temperature rise.

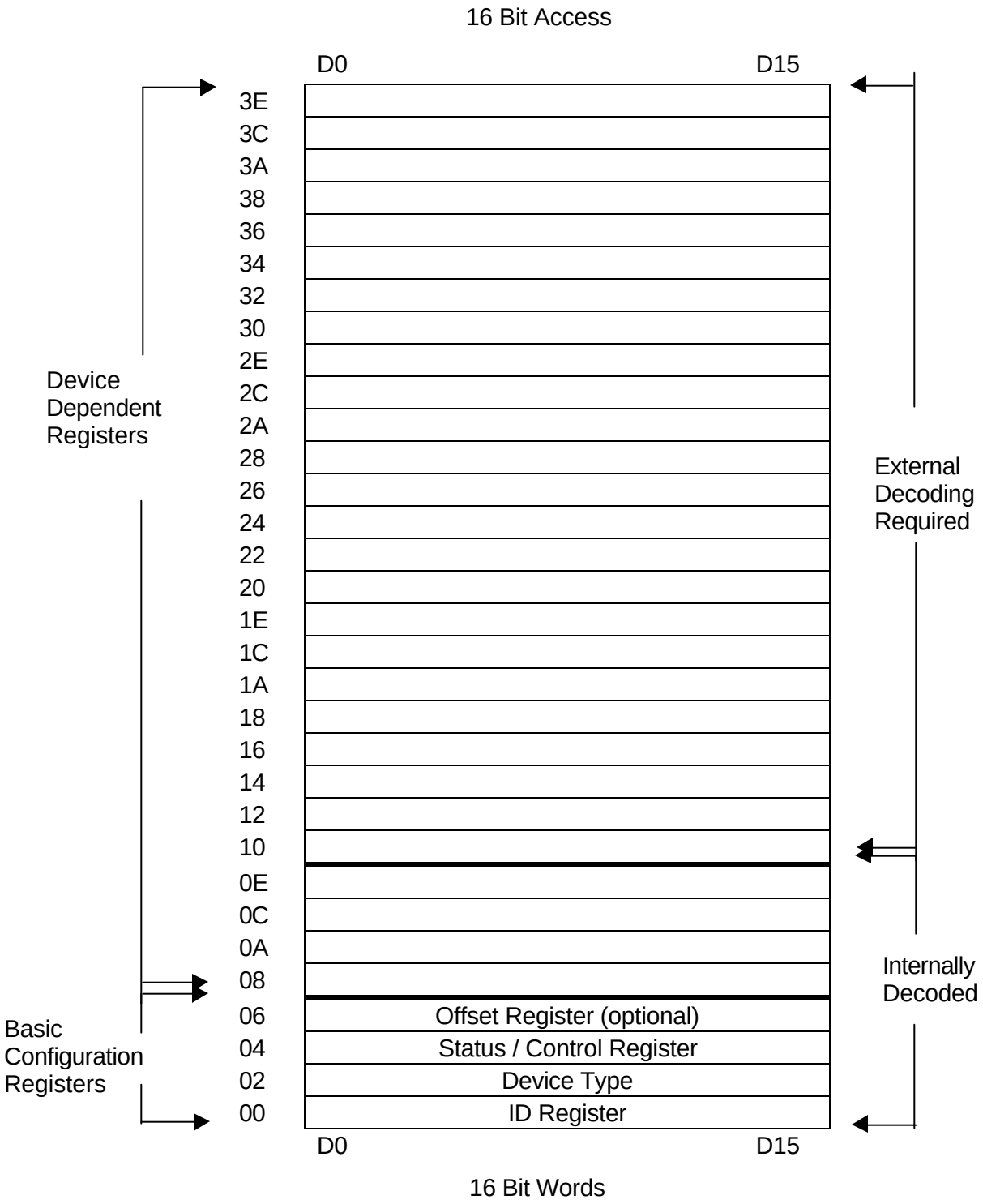


Figure 3-11, 7064R Register Map – 16 bit access

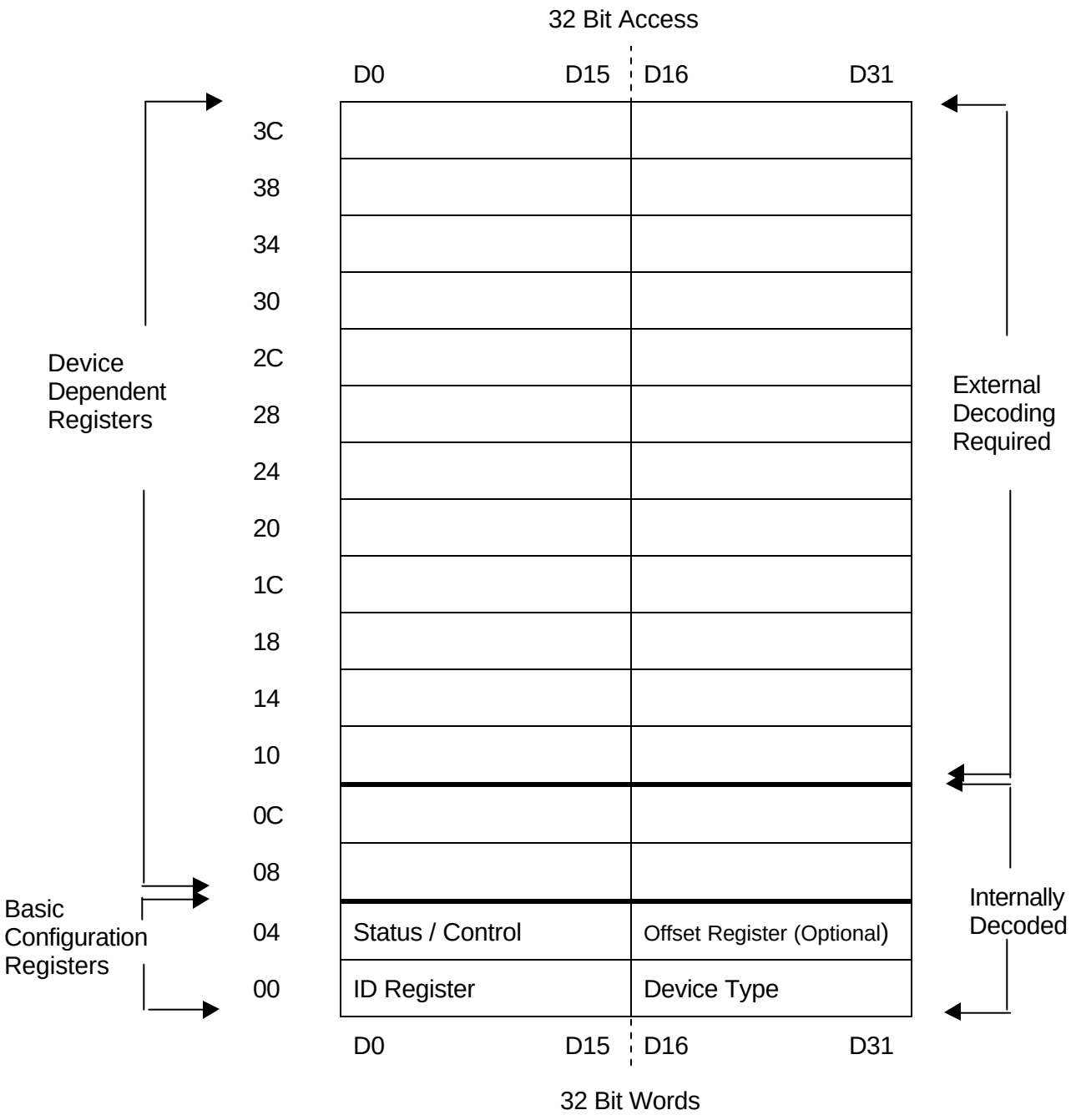
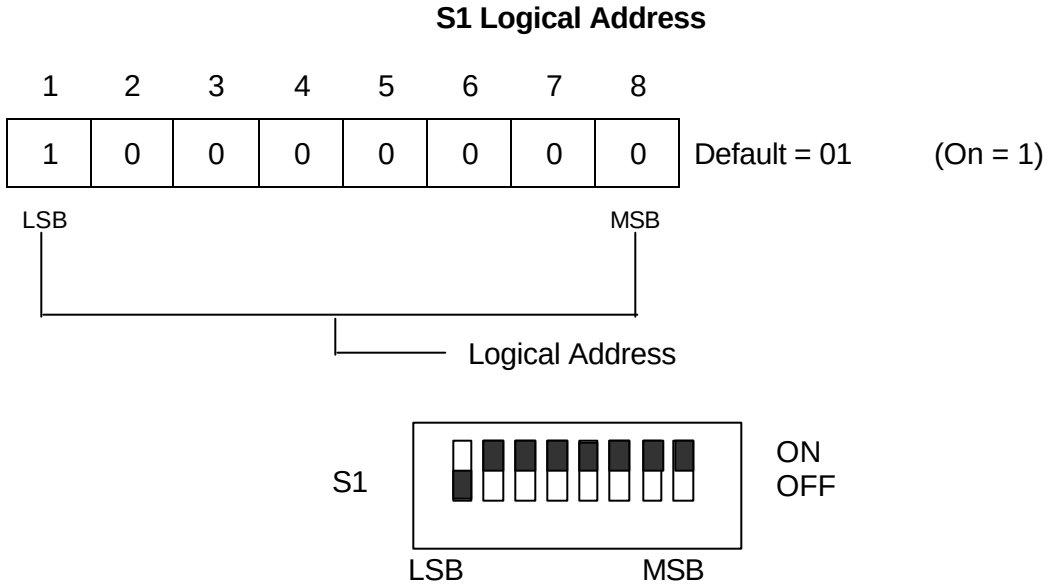


Figure 3-12, 7064R Register Map – 32 bit access



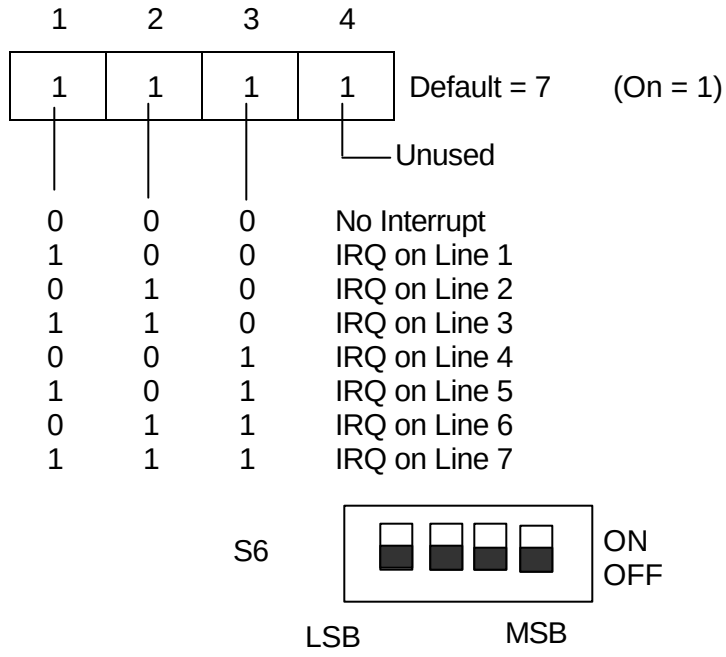
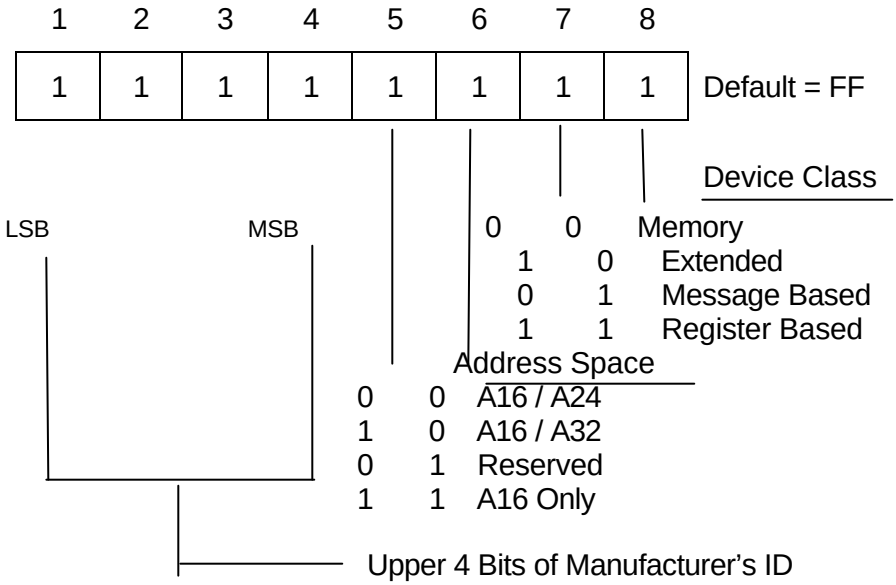
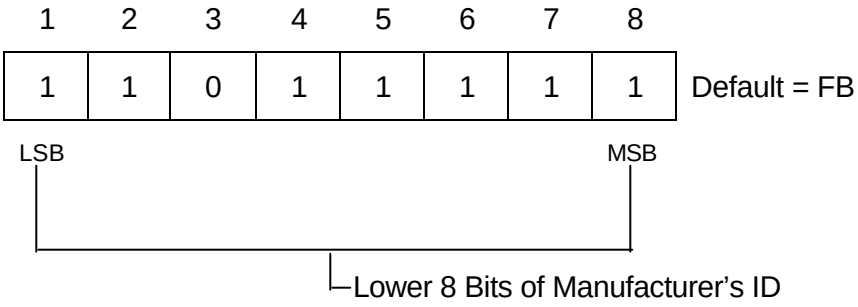


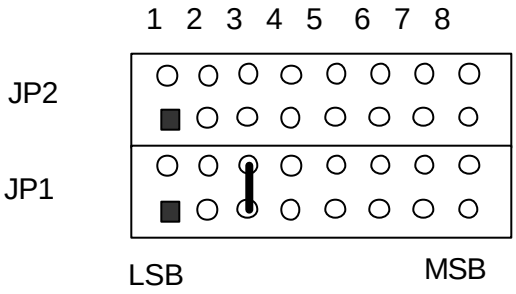
Figure 3-13, 7064R Logical Address and Interrupt Switches

JP2 ID Register (Upper Half)



JP1 ID Register (Lower Half)

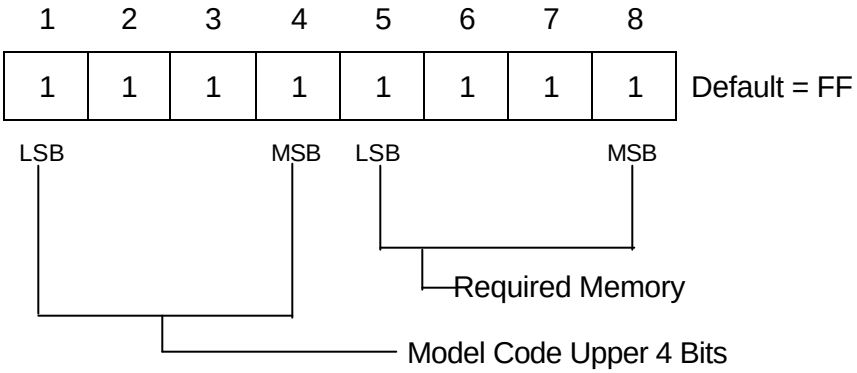




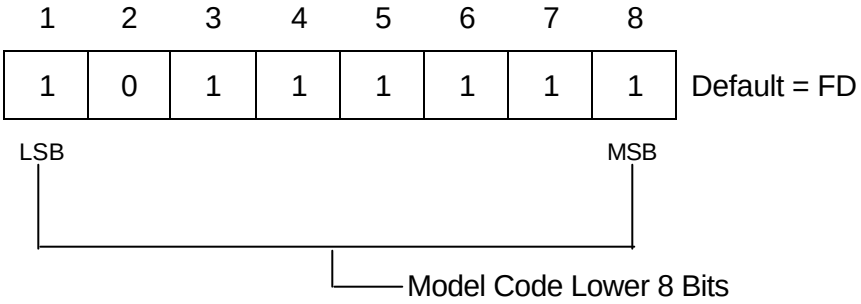
OPEN = 1
SHORT = 0

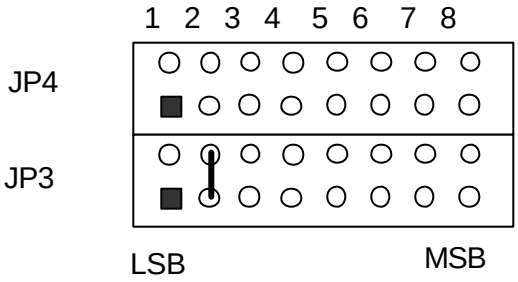
Figure 3-14, ID register Jumpers

JP4 Device Type Register (Upper Half)



JP3 Device Type Register (Lower Half)



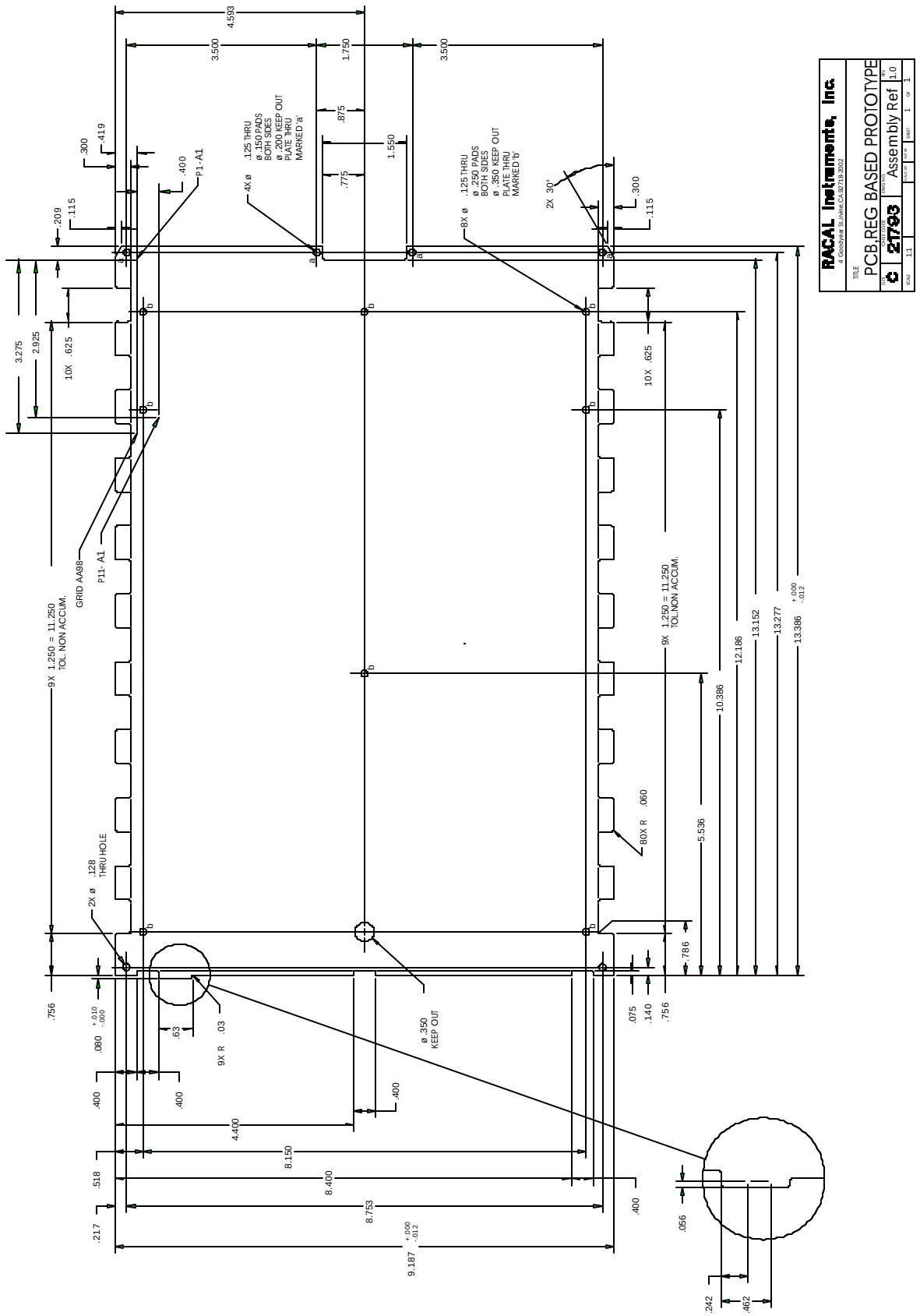


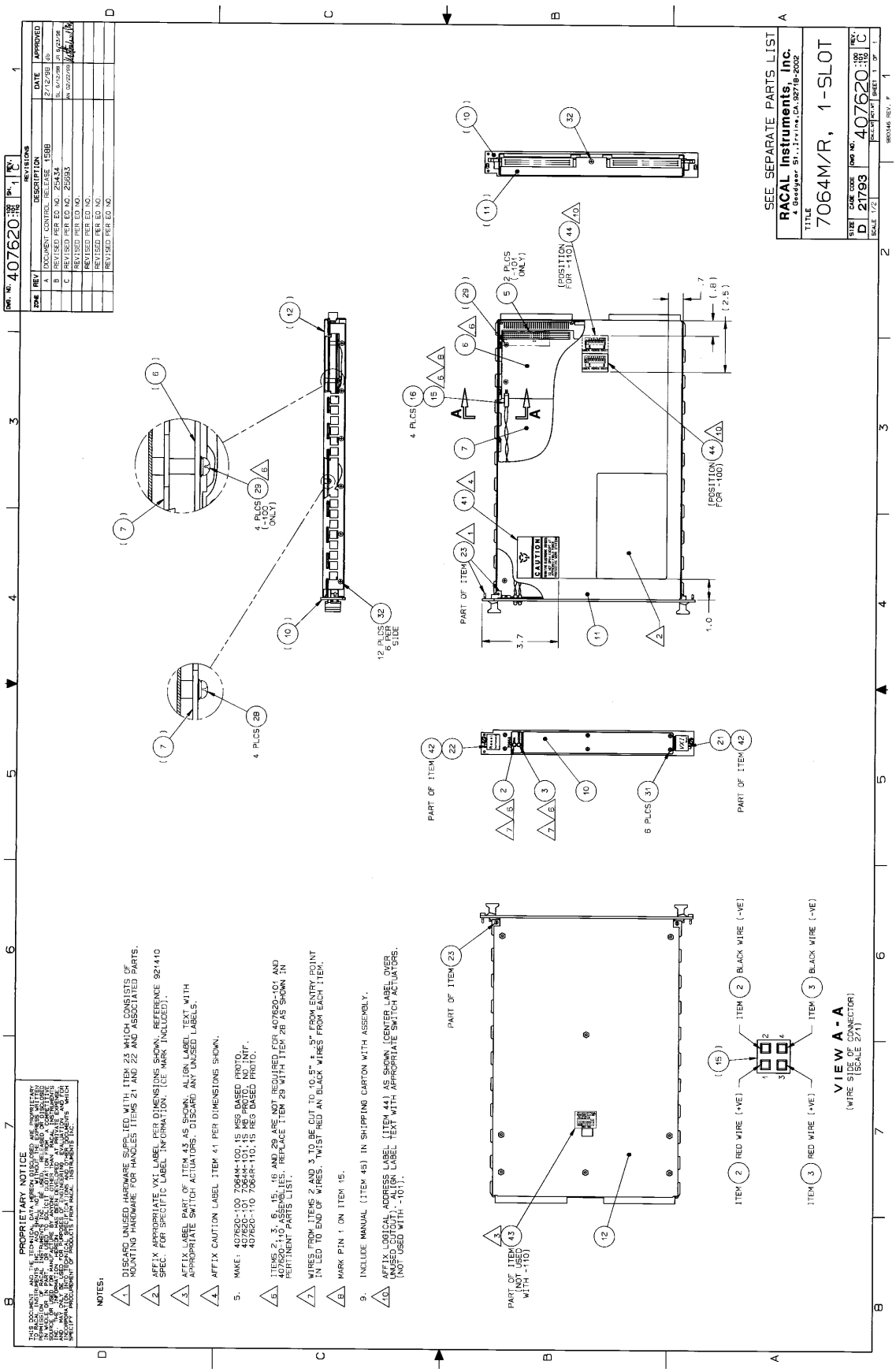
OPEN = 1
SHORT = 0

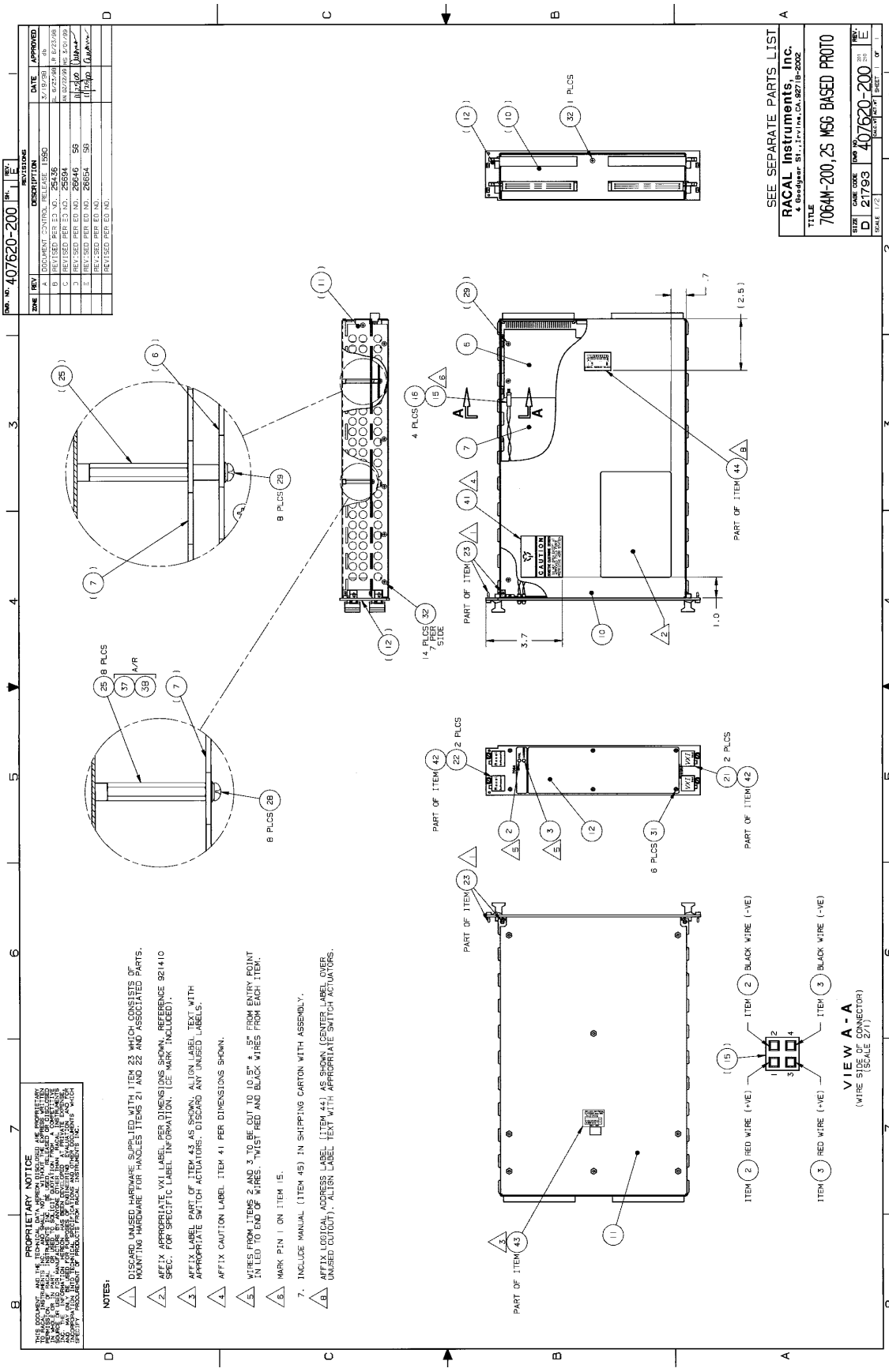
Figure 3-15, Device Type Register Jumpers

Chapter 4
DRAWINGS

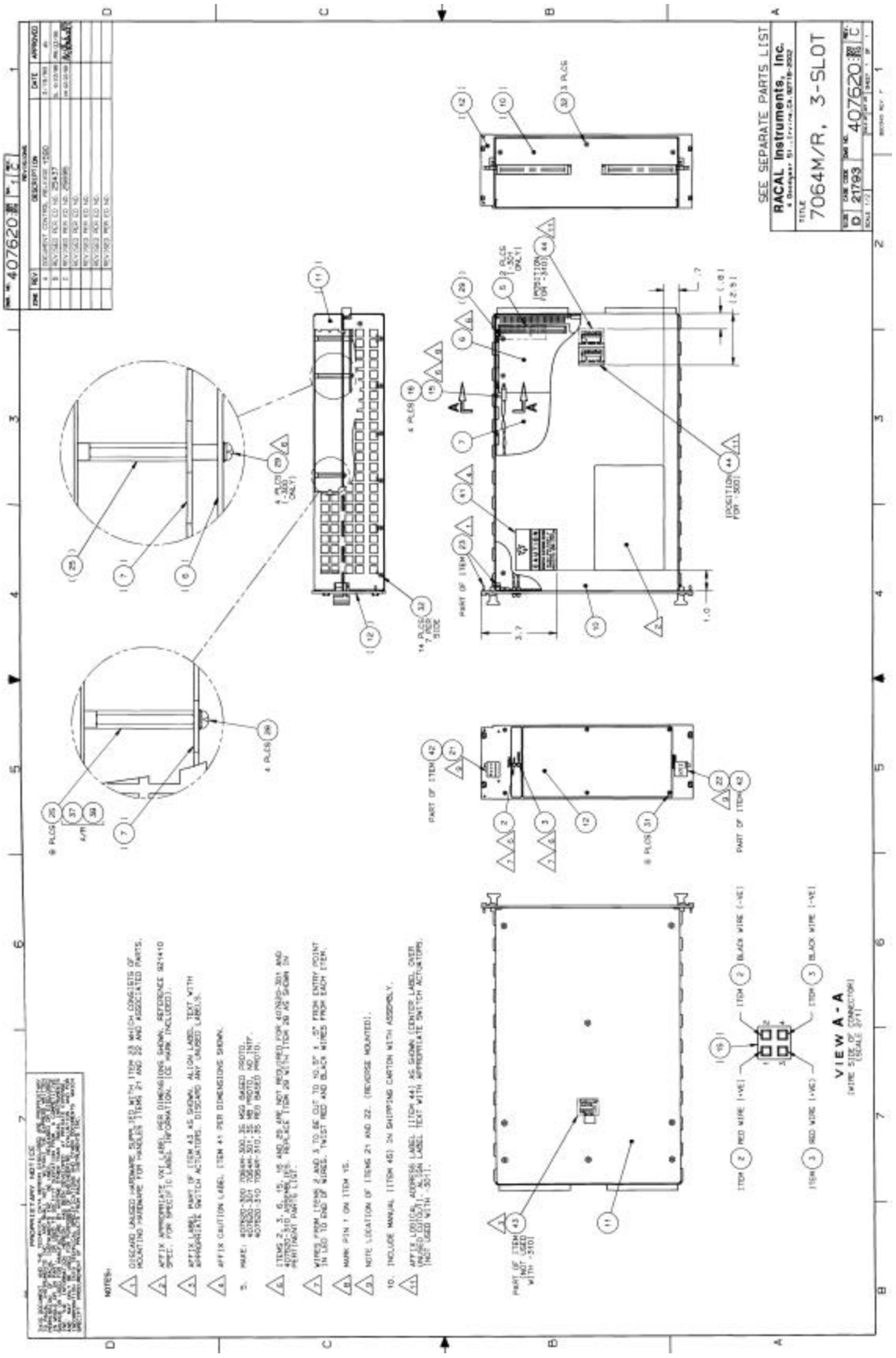
Assembly Ref.	PCB, Reg Based Prototype	4-2
407620-110	Final Assy, 7064R, 1-Slot	4-3
407620-210	Final Assy, 7064R, 2-Slot	4-4
407620-310	Final Assy, 7064R, 3-Slot	4-5
405123	PCB Assy, Reg Based Prototype	4-6
405123-119	Bare Board Prototype	4-8
435123	Schematic, 7064R, Reg Based Proto	4-9


RACAL Instruments, Inc.
4 Goodyear St.Irvine,CA.92718-2002
TITLE
PCB,REG BASED PROTOTYPE
Assembly Ref
1.0
2793
4.593
3.500
1.750
3.500
.419
.300
.400
P1-A1
.209
.115
4X ø .125 THRU ø .150 PADS BOTH SIDES ø .200 KEEP OUT PLATE THRU MARKED 'a'
.875
1.550
.775
8X ø .125 THRU ø .250 PADS BOTH SIDES ø .350 KEEP OUT PLATE THRU MARKED 'b'
2X 30°
.300
.115
3.275
2.925
10X .625
10X .625
GRID AA98
P11- A1
9X 1.250 = 11.250 TOL.NON ACCUM.
9X 1.250 = 11.250 TOL.NON ACCUM.
10.386
12.186
13.152
13.277
13.386
80X R .060
5.536
.786
2X ø .128 THRU HOLE
.756
.080
.063
9X R .03
ø .350 KEEP OUT
.075
.140
.756
.400
.400
.400
4.400
8.150
8.400
8.753
.518
.217
9.187
.056
.242
.462

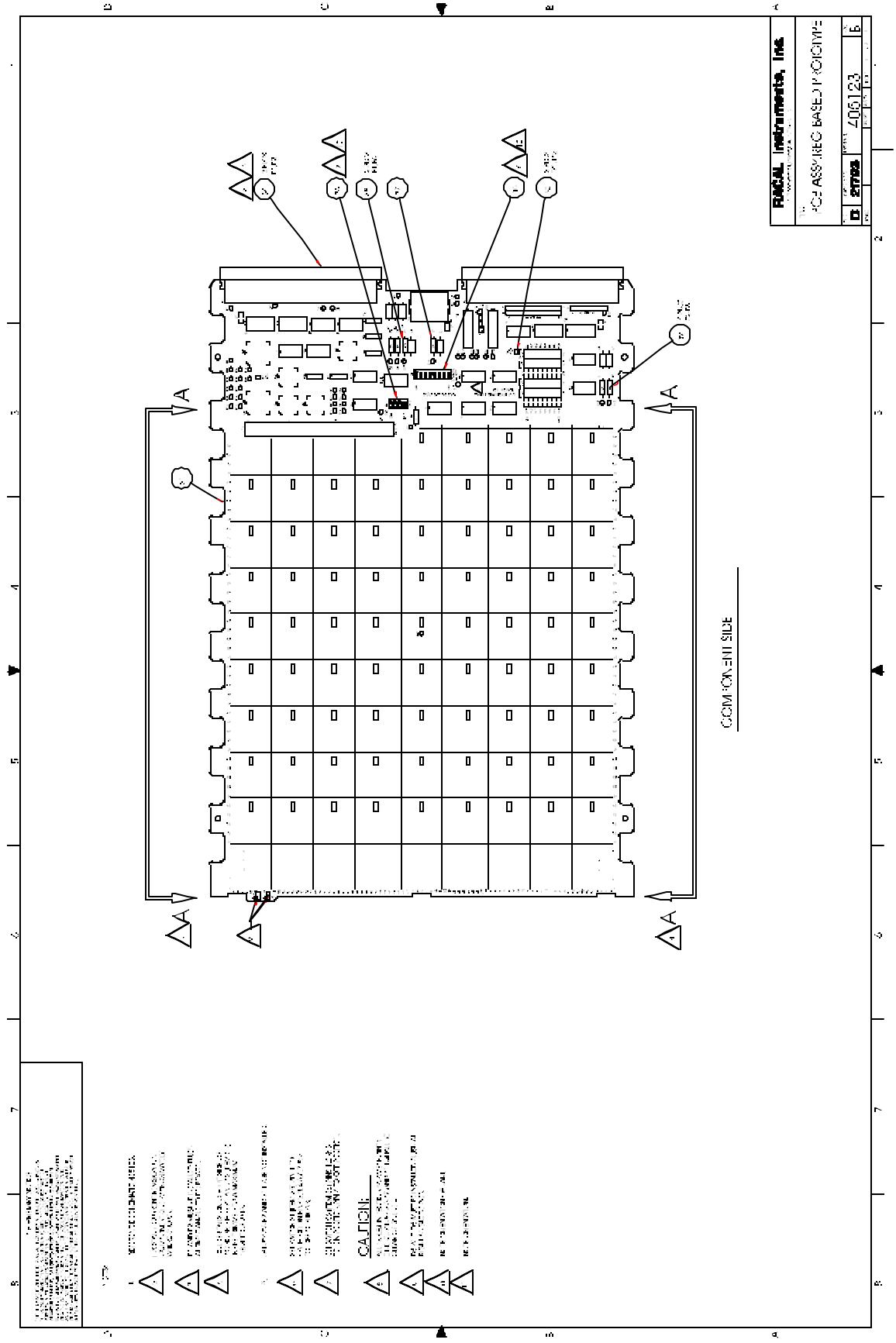

DWG. NO. 407620-100 thru -110 REV. C
REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPROVED
A | DOCUMENT CONTROL RELEASE 1598 | 2/12/98
B | REVISED PER EO NO. 25434 | 5/12/98
C | REVISED PER EO NO. 25983 | 02/23/99
REVISED PER EO NO.
REVISED PER EO NO.
REVISED PER EO NO.
REVISED PER EO NO.
PROPRIETARY NOTICE
NOTES:
1. DISCARD UNUSED HARDWARE SUPPLIED WITH ITEM 23 WHICH CONSISTS OF MOUNTING HARDWARE FOR HANDLES ITEMS 21 AND 22 AND ASSOCIATED PARTS.
2. AFFIX APPROPRIATE VXI LABEL PER DIMENSIONS SHOWN, REFERENCE 921410 SPEC. FOR SPECIFIC LABEL INFORMATION. (CE MARK INCLUDED).
3. AFFIX LABEL PART OF ITEM 43 AS SHOWN. ALIGN LABEL TEXT WITH APPROPRIATE SWITCH ACTUATORS. DISCARD ANY UNUSED LABELS.
4. AFFIX CAUTION LABEL ITEM 41 PER DIMENSIONS SHOWN.
5. MAKE: 407620-100 7064M-100, 1S MSG BASED PROTO.
407620-101 7064M-101, 4S MB PROTO, NO INTF.
407620-110 7064R-110, 1S RES BASED PROTO.
6. ITEMS 2, 3, 6, 15, 16 AND 29 ARE NOT REQUIRED FOR 407620-101 AND 407620-110 ASSEMBLIES. REPLACE ITEM 29 WITH ITEM 28 AS SHOWN IN PERTINENT PARTS LIST.
7. WIRES FROM ITEMS 2 AND 3 TO BE CUT TO 10.5" ± .5" FROM ENTRY POINT IN LED TO END OF WIRES. TWIST RED AN BLACK WIRES FROM EACH ITEM.
8. MARK PIN 1 ON ITEM 15.
9. INCLUDE MANUAL (ITEM 45) IN SHIPPING CARTON WITH ASSEMBLY.
10. AFFIX LOGICAL ADDRESS LABEL (ITEM 44) AS SHOWN (CENTER LABEL OVER UNUSED CUTOUT). LABEL TEXT WITH APPROPRIATE SWITCH ACTUATORS. (NOT USED WITH -101).
SEE SEPARATE PARTS LIST
RACAL Instruments, Inc.
4 Goodyear St., Irvine, CA. 92718-2002
TITLE
7064M/R, 1-SLOT
SIZE D | CAGE CODE 21793 | DWG NO. 407620 | REV. C
SCALE 1/2 | SHEET 1 OF 1
VIEW A - A
(WIRE SIDE OF CONNECTOR)
(SCALE 2/1)
ITEM (2) RED WIRE (+VE)
ITEM (3) RED WIRE (+VE)
ITEM (2) BLACK WIRE (-VE)
ITEM (3) BLACK WIRE (-VE)
4 PLCS (-100 ONLY)
4 PLCS
12 PLCS 6 PER SIDE
2 PLCS (-101 ONLY)
[POSITION FOR -110]
[POSITION FOR -100]
PART OF ITEM
6 PLCS
PART OF ITEM (NOT USED WITH -100)

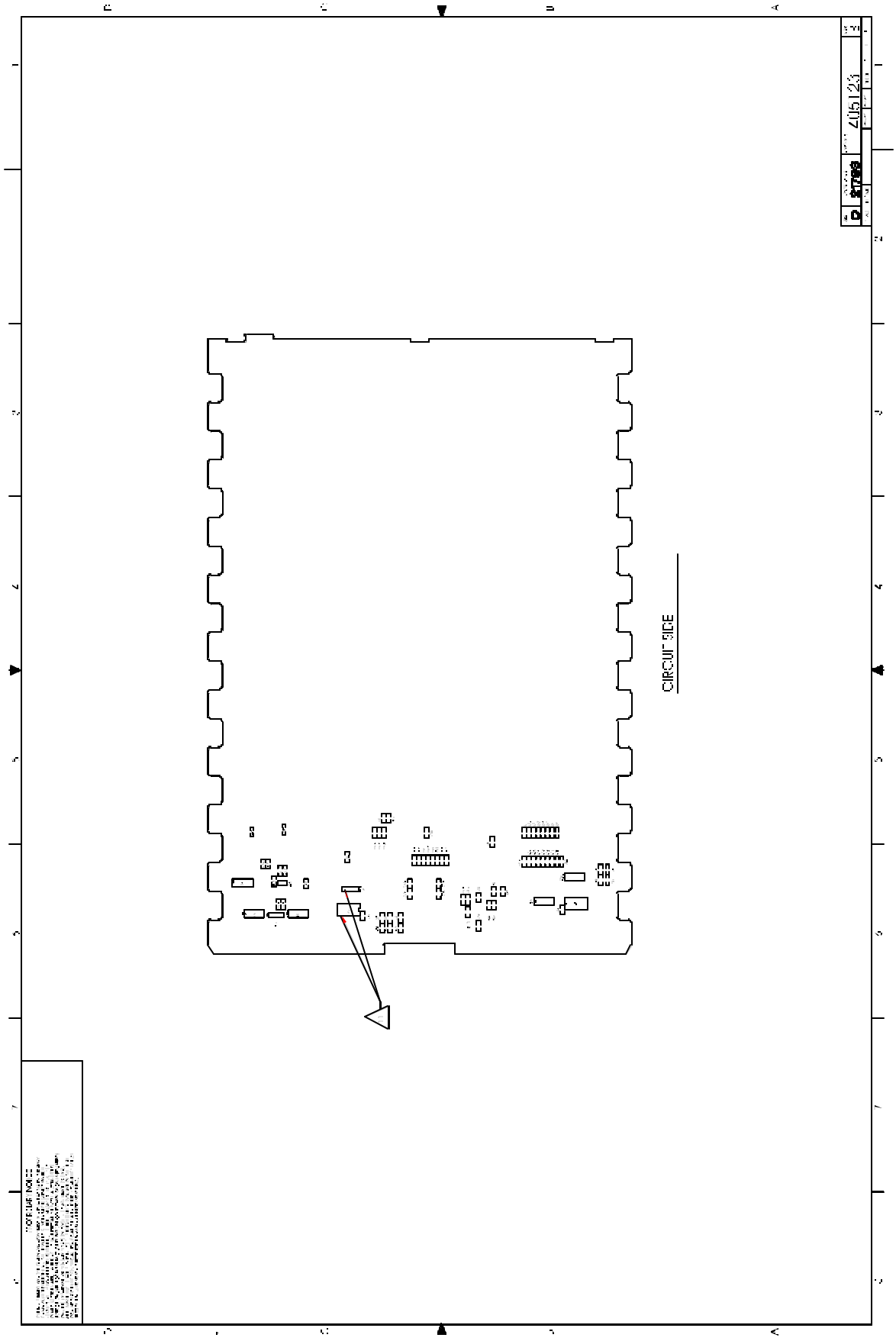


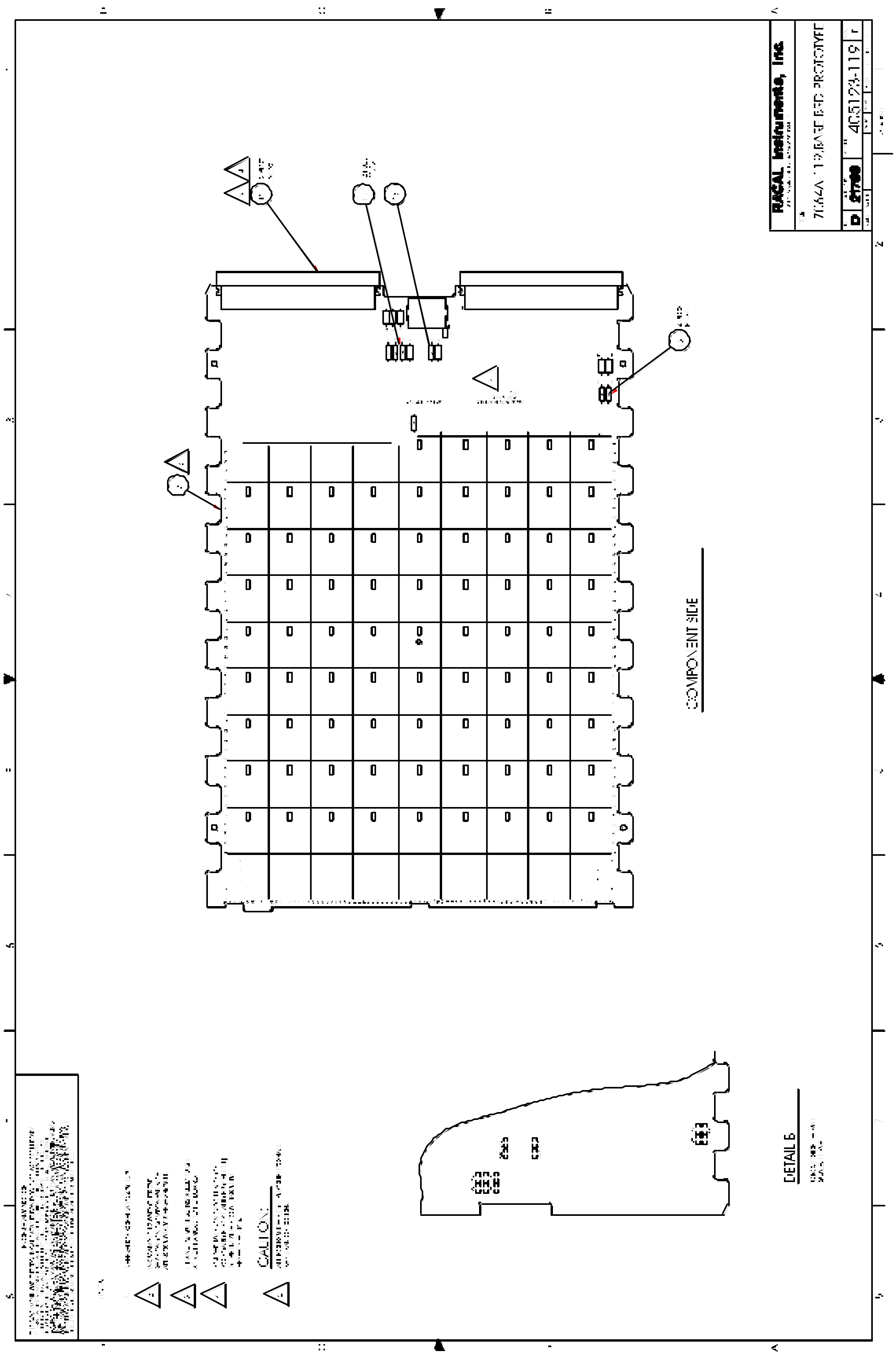
Revised 2-15-02



Revised 2-15-02


RACAL Instruments, Ltd.
PCI ASSY REC BASEJ PROTYPE
406123
COMPONENT SIDE
CAUTION


CIRCUIT SIDE


RACAL Instruments, Inc.
COMPONENT SIDE
DETAIL B
CAUTION

DWG. NO. 435123		SH. 1	REV. A
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	DOCUMENT CONTROL RELEASE		
	REVISED PER EC NO.		
	REVISED PER EC NO.		
	REVISED PER EC NO.		

NOTES:

1. RESISTOR VALUES ARE IN OHMS, 1/4W, 5% UNLESS OTHERWISE SPECIFIED.
2. CAPACITOR VALUES ARE IN UF, 50V, 10% UNLESS OTHERWISE SPECIFIED.
3. ⚠ COMPONENTS IN DASHED LINES ARE NOT INSTALLED.
4. ⚠ THE CIRCUITRY ASSOCIATED WITH THE PARTS SHOWN IN DASHED OUTLINE IS PROPRIETARY TO RACAL INSTRUMENTS INC. AND IS NOT INCLUDED IN THIS DRAWING.

POINT	SIGNAL	SHEET	POINT	SIGNAL	SHEET
E1	+5V	3	E24	SYSFAILINH	9
E2	+12V	3	E25	DEVCTRL2	9
E3	ACFAIL-	2	E26	DEVCTRL3	9
E4	SERCLK	2	E27	DEVCTRL4	9
E5	SERDAT-	2	E28	DEVCTRL5	9
E6	-12V	3	E29	DEVCTRL6	9
E7	CLK10+	2	E30	A24/A32EN	9
E8	CLK10-	2	E31	USE5VSEALED	9
E9	+5VSTDBY	2	E32	EC_TRG0-	3
E10	+24V	3	E33	EC_TRGIN0-	3
E11	SUMBUS	2	E34	EC_TRGIN0	3
E12	-24V	3	E35	EC_TRGIN1-	3
E13	-5.2V	3	E36	EC_TRGIN1	3
E14	-2V	3	E37	EC_TRG1-	3
E15	STATREGEN-9	9	E38	MYSTACK-	6
E16	PASSED	9	E39	MYSTACK-	6
E17	READY	9	E40	IRQEN-	6
E18	DEVSTAT3	9	E41	PERR	2
E19	DEVSTAT	9	E42	INSTRST-	7
E20	DEVSTAT4	9	E43	CHASSIS	1
E21	DEVSTAT5	9	E44	RDEN-	6
E22	CTRLRSTEN	9	E45	WREN	6
E23	SRESET	9			

MASTER SHEET

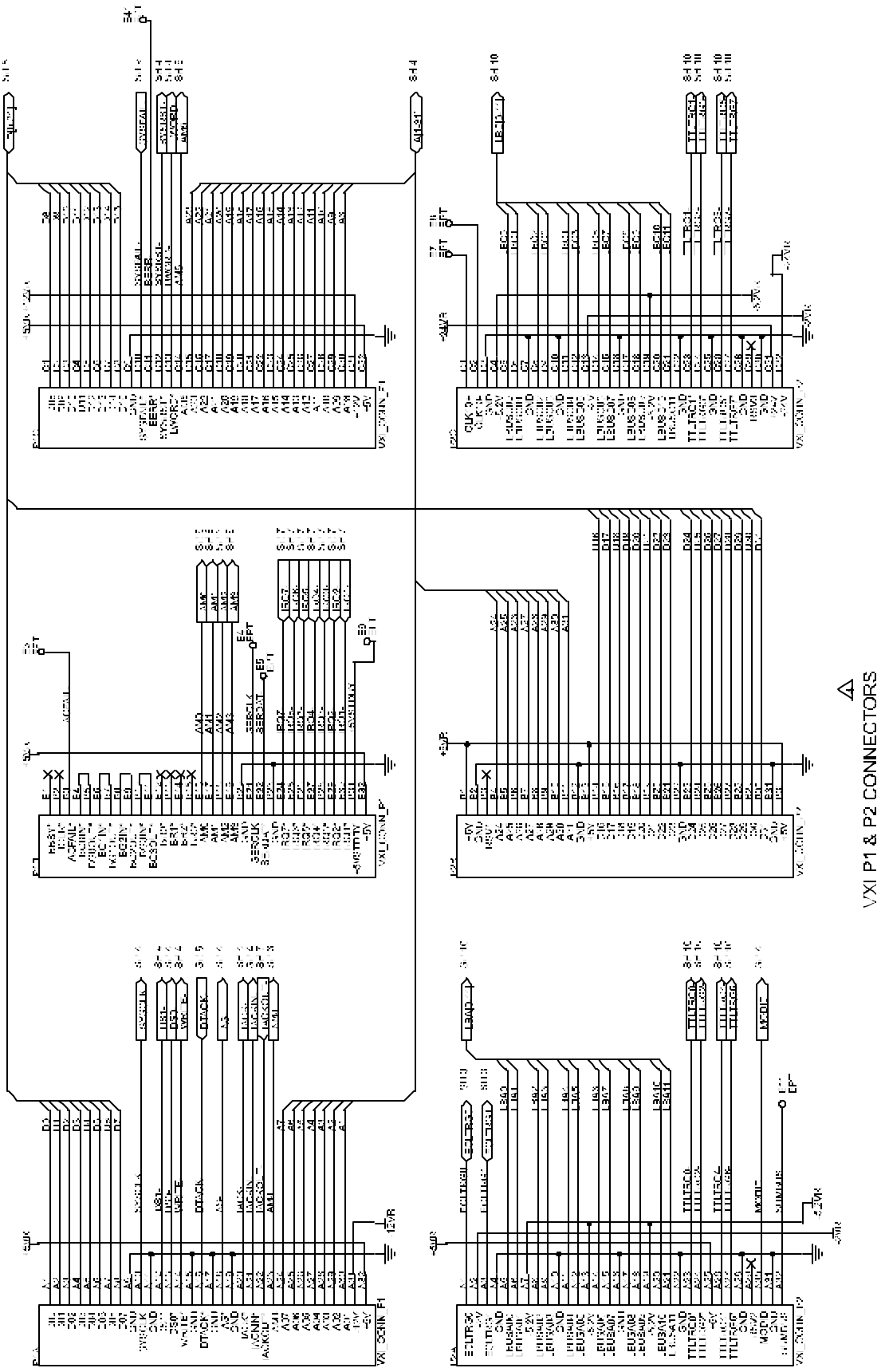
DEVICE TYPE	REFERENCE DESIGNATOR	POWER PINS VCC	GND	VEE
16L8C-25 (231575-001)	U12	20	10	
16L8C-25 (231575-001)	U15	20	10	
16L8C-25 (231575-003)	U24	20	10	
16L8C-25 (231575-004)	U29	20	10	
22V10-25 (231576-001)	U25	24	12	
22V10-25 (231576-002)	U28	24	12	
74FCT244	U1,U4,U7,U8,U9,U11	20	10	
74F245	U5,U6	20	10	
74ALS641-1	U27	20	10	
74FCT652	U2,U3,U10,U13	24	12	
74HCT32	U20	14	7	
74ACT04	U22	14	7	
74HCT30	U30	14	7	
74HCT138	U32	16	8	
74HCT244	U18,U19,U21,U31,U42	20	10	
74HCT273	U17	20	10	
74F32	U27	14	7	
74HCT688	U14,U29	20	10	
74HCT74	U33	14	7	
74S38	U16	14	7	
10H116	U40		-5.2	8
10H123	U39		-5.2	8
LM555C	U35	8		

HIGHEST REF DES
C30
D8
E45
F7
JP7
L8
P11
R101
S6
TP2
U42
Z10

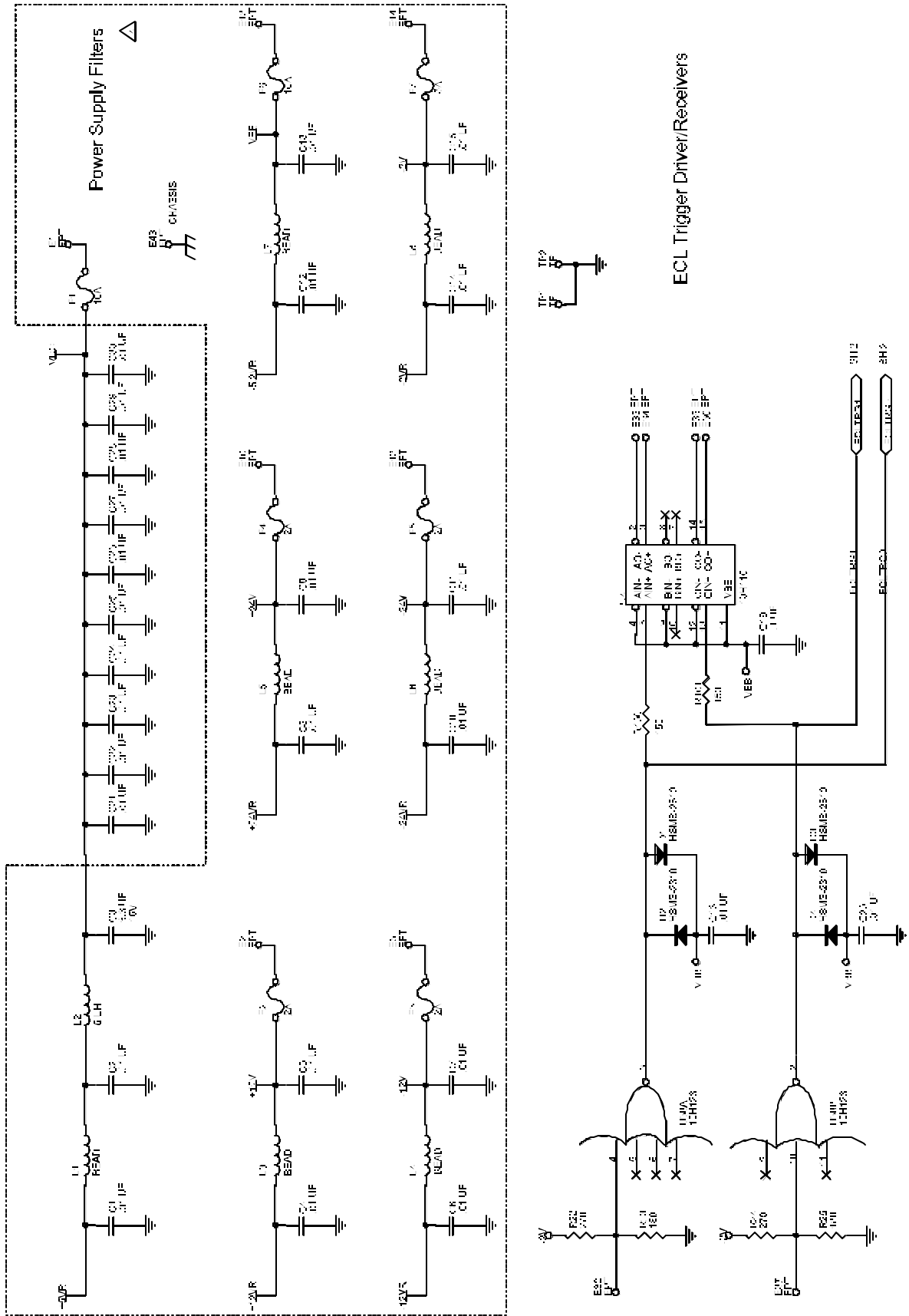
RACAL Instruments, Inc.
4 Goodyear St., Irvine, CA. 92618

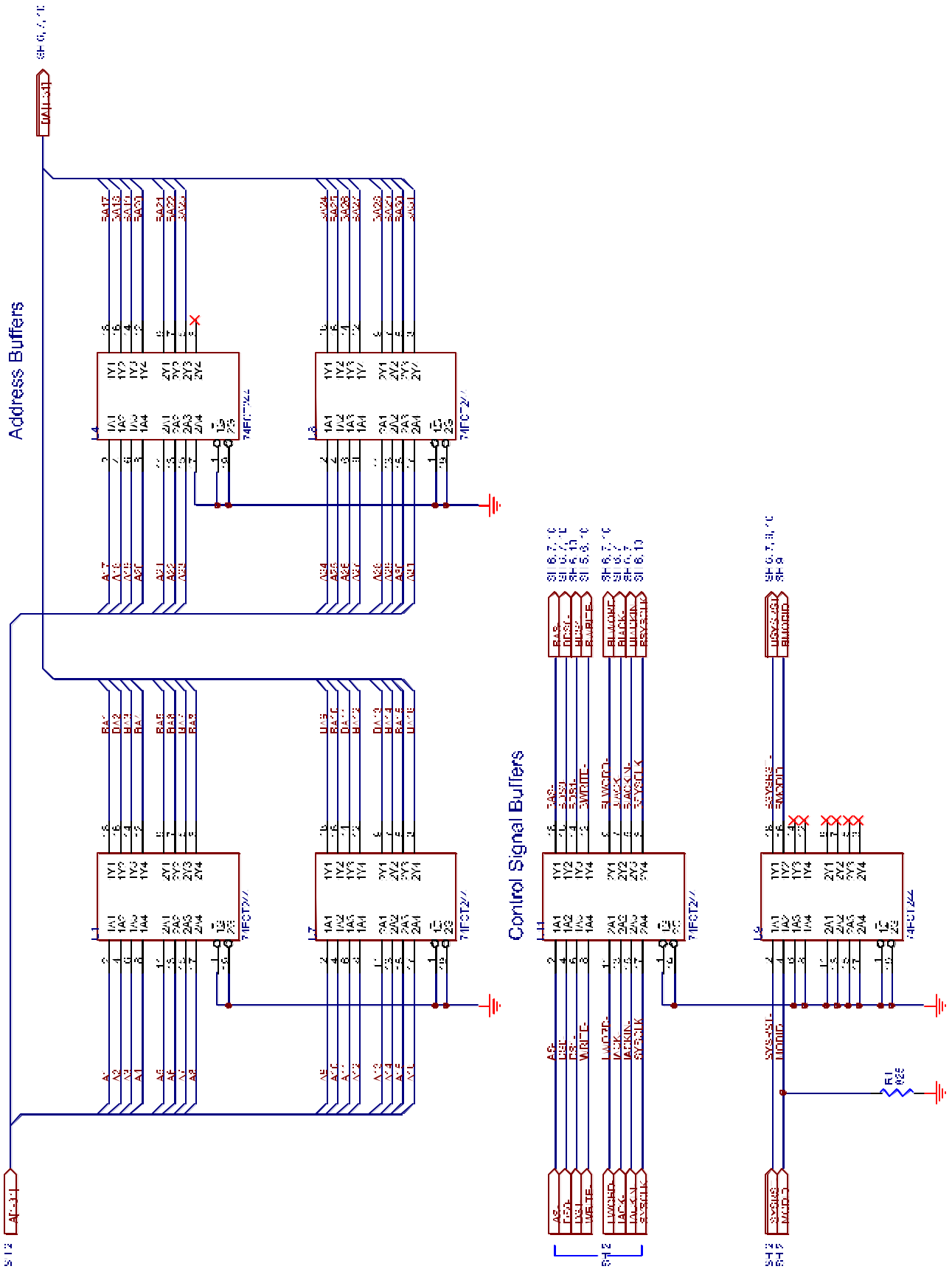
TITLE
SCHEMATIC, REG BASED PROTOTYP

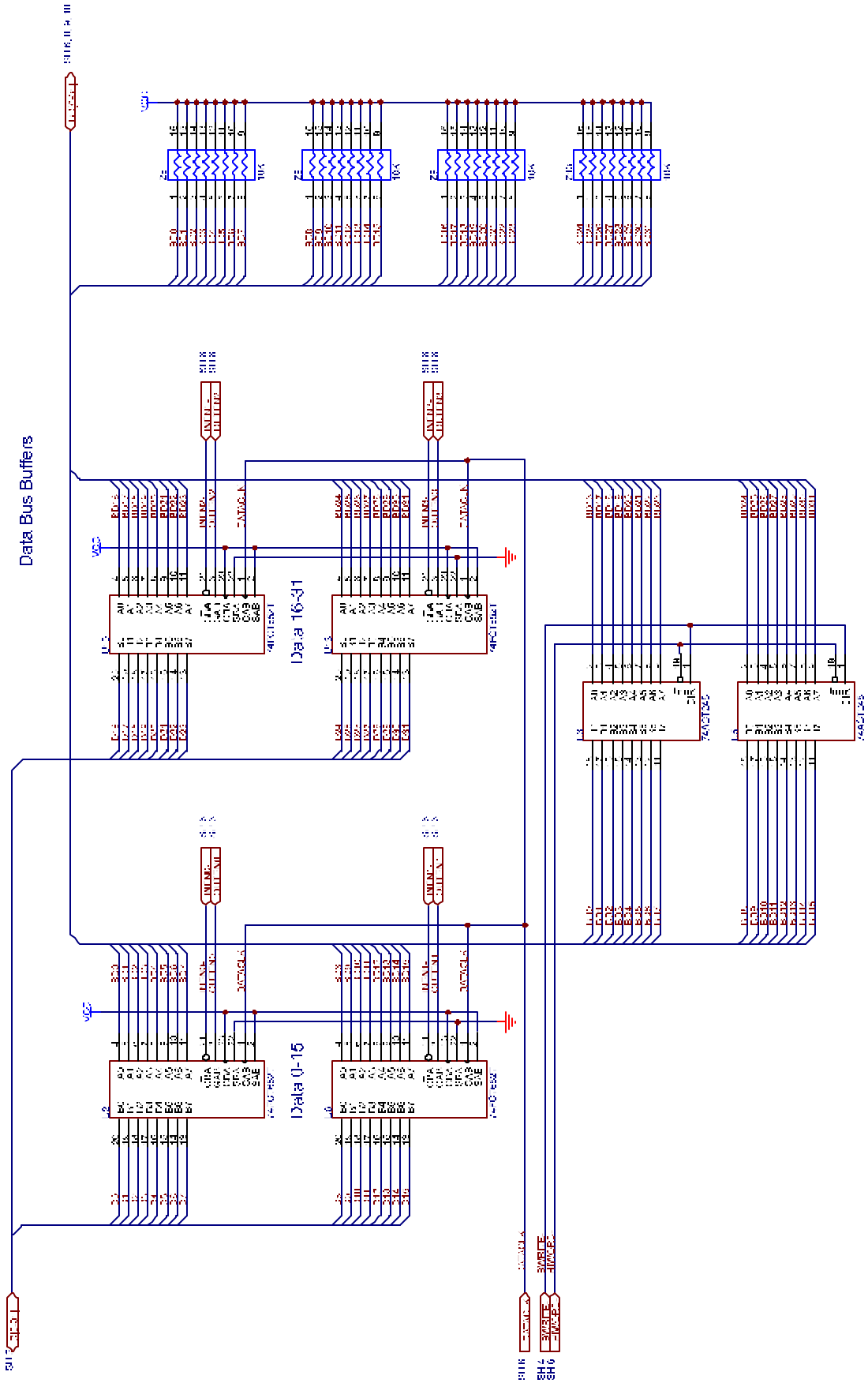
SIZE	CAGE CODE	DWG NO.	REV.
B	21793	435123	B
SCALE NONE		14-Nov-1997	SHEET 1 OF 10

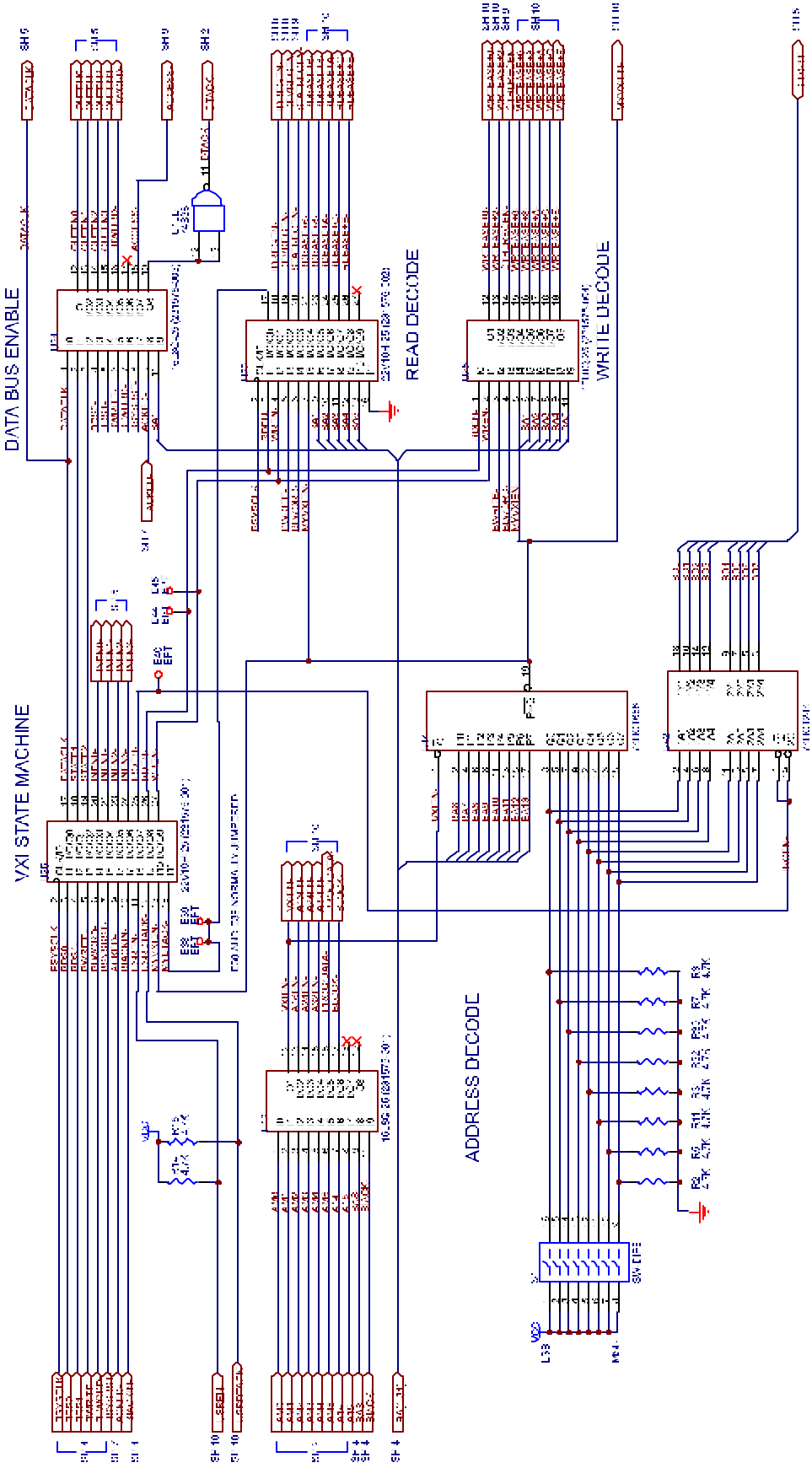


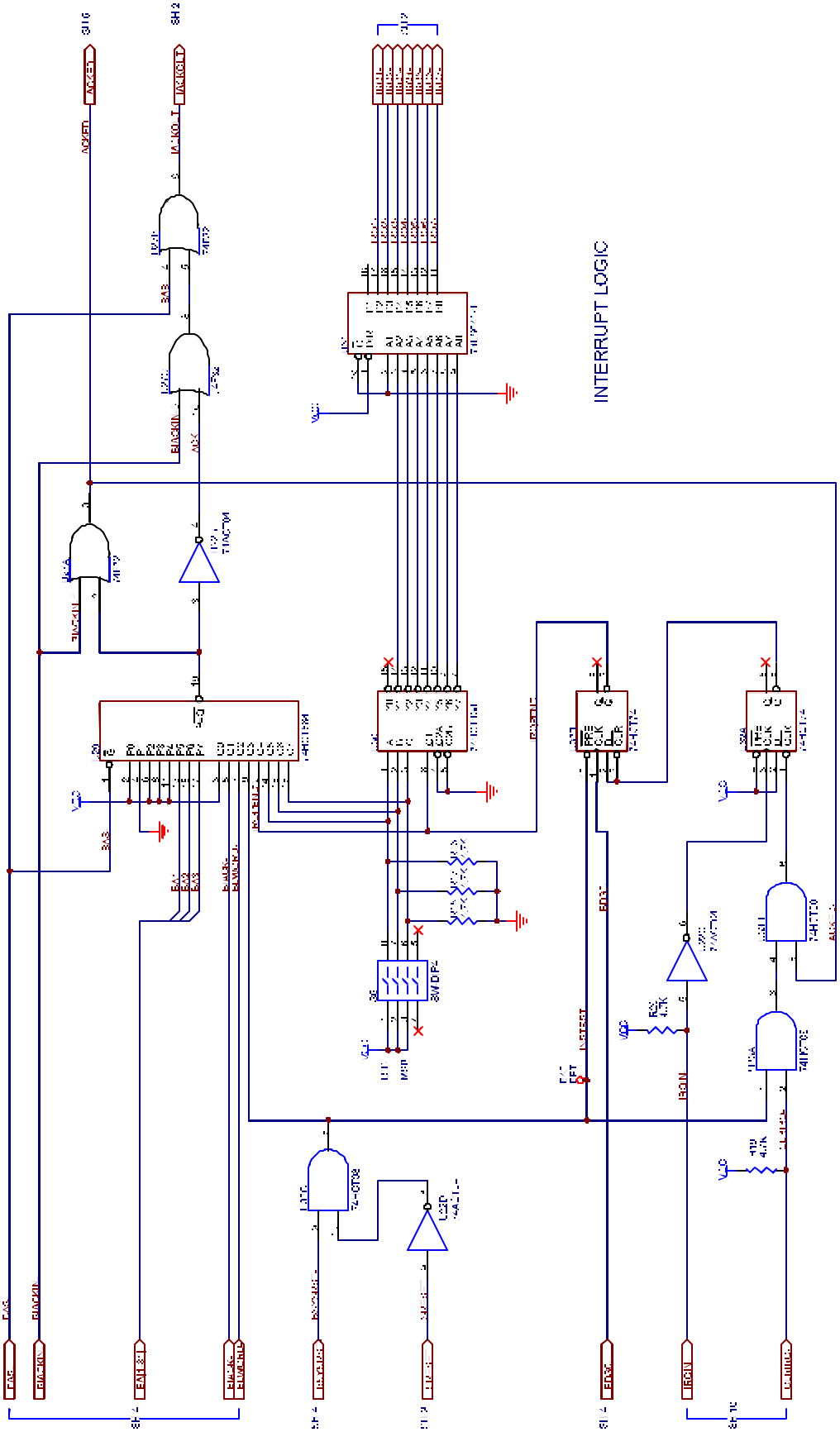
VXI P1 & P2 CONNECTORS

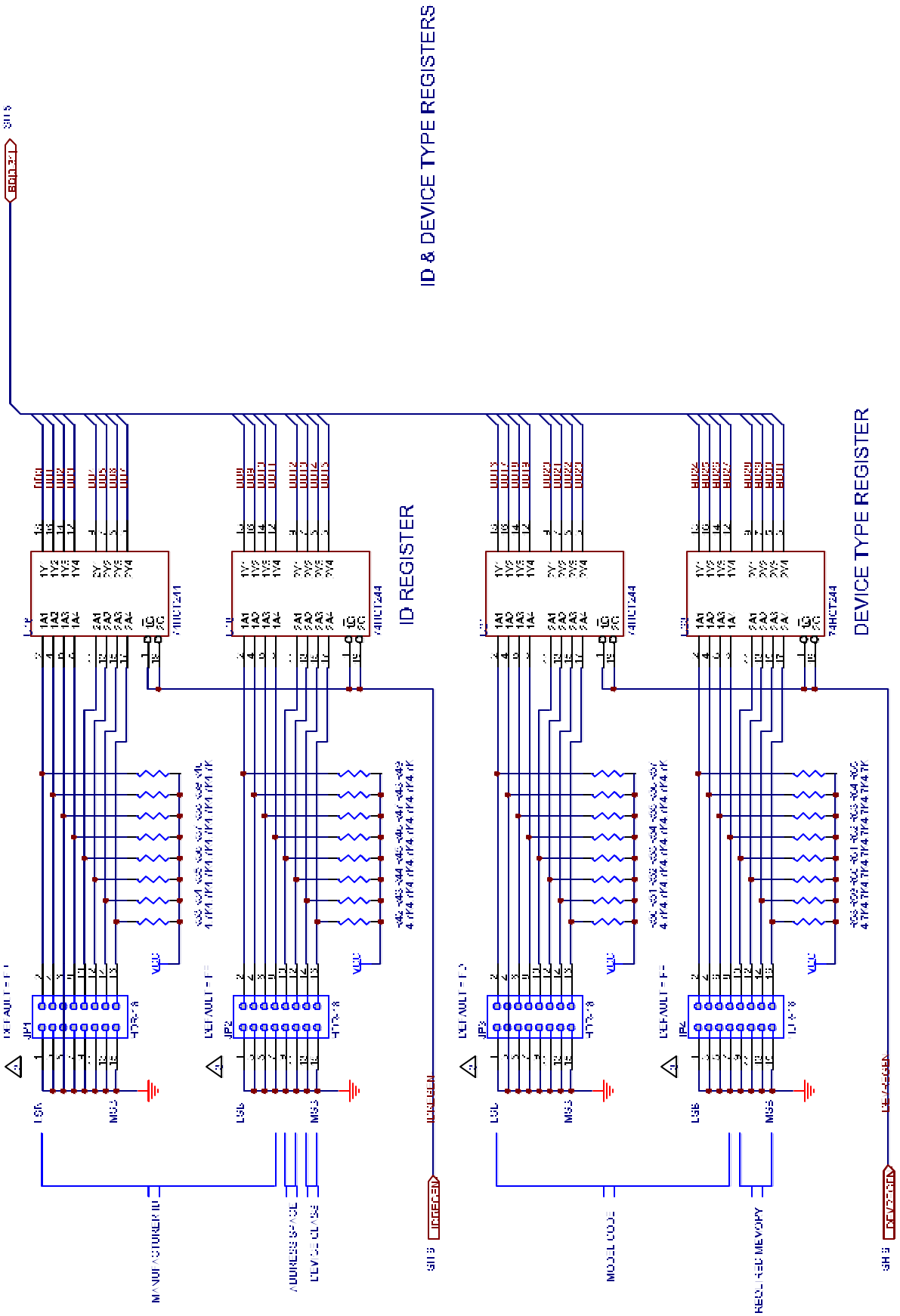

Power Supply Filters
CHASSIS
ECL Trigger Driver/Receivers

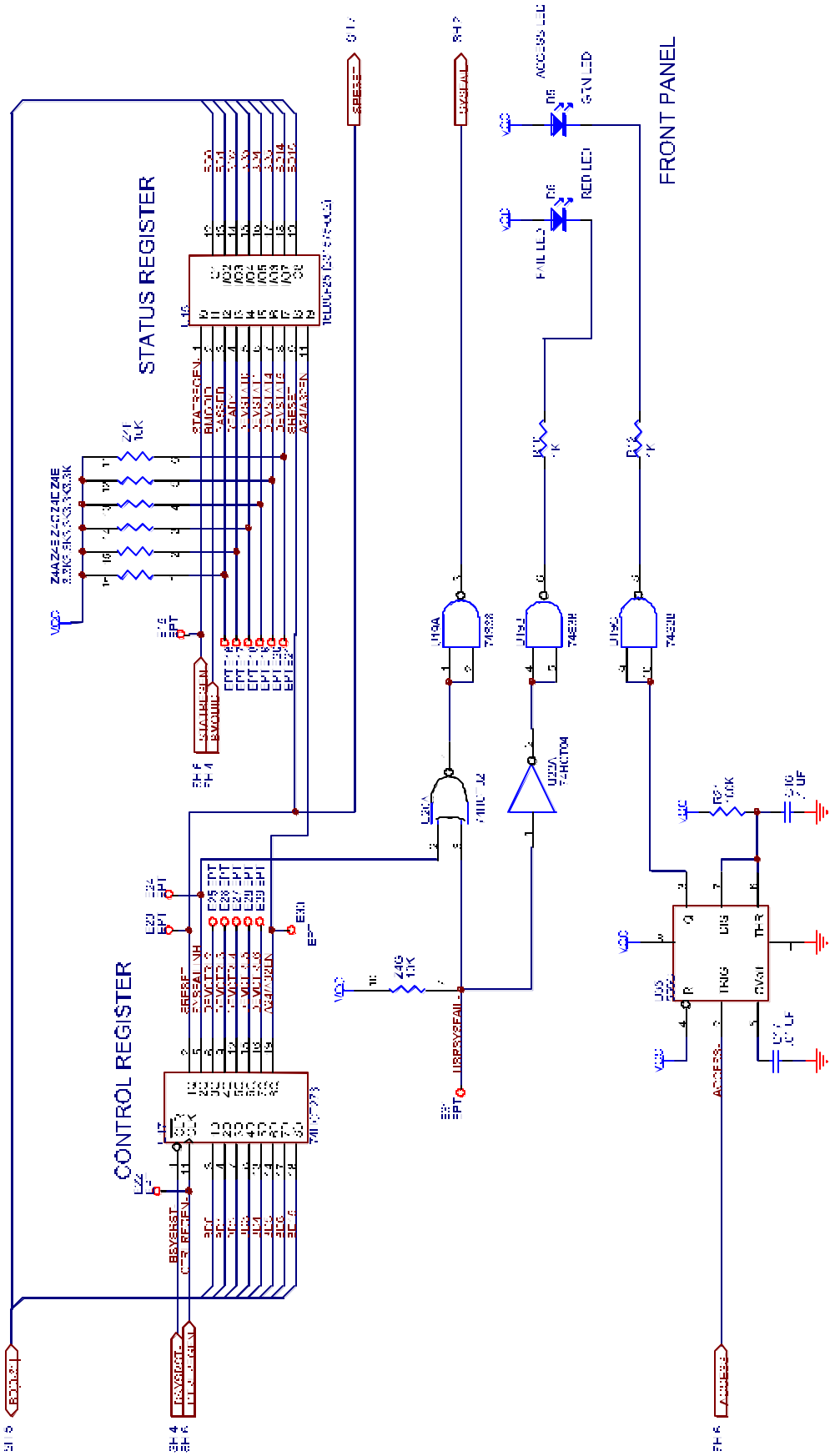

Address Buffers
Control Signal Buffers

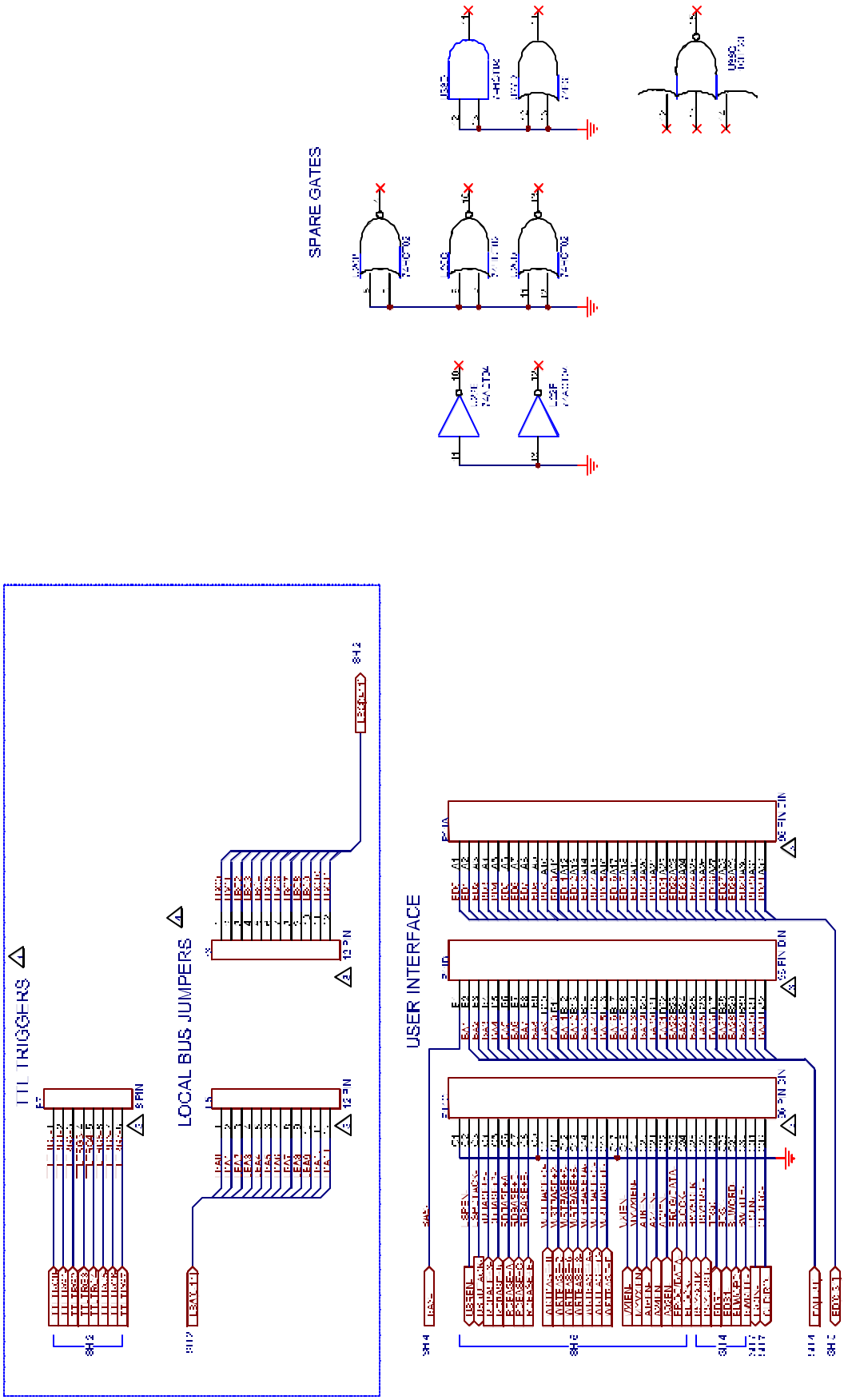

Data Bus Buffers
Data 16-31
Data 0-15


DATA BUS ENABLE
READ DECODE
WRITE DECODE
VXI STATE MACHINE
ADDRESS DECODE


INTERRUPT LOGIC


ID & DEVICE TYPE REGISTERS
ID REGISTER
DEVICE TYPE REGISTER


STATUS REGISTER
CONTROL REGISTER
FRONT PANEL


SPARE GATES
TTL TRIGGERS
LOCAL BUS JUMPERS
USER INTERFACE

Chapter 5
PARTS LIST

407620-110	Final Assembly, 7064R-110,1S Reg Based Proto	5-3
407620-210	Final Assembly, 7064R-210,2S Reg Based Proto	5-4
407620-310	Final Assembly, 7064R-310,3S Reg Based Proto	5-5
405123	PCB Assy, Reg Based Prototype	5-6
407620-119	Reg Based Bare Brd.	5-7
405123-119	PCB Assy, Bare Board Prototype	5-8

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ENGINEERING PARTS LIST

Assembly 407620-110
Description 7064R-110, 1S REG BASED PROTO-N
EA

Low Level Code 01
Revision Date 1999-03-04
Revision C

#	Component	Description	UM	Qty Reqd	Txt
	SP-152-CA	1260 CARD PAK	EA	1.000	
7	405123	PCB ASSY, REG BASED PROTOTYPE	EA	1.000	
10	456421	PANEL, FRONT, 7064M/R, 1-SLOT	EA	1.000	
11	456422	COVER, TOP, 7064A, 1-SLOT	EA	1.000	
12	456423	COVER, BOTTOM, 7064A, 1-SLOT	EA	1.000	
21	611264	HANDLE-EXT-BOT	EA	1.000	
22	611265	HANDLE-EXT-TOP	EA	1.000	
23	611266	MOUNTING HDW, HANDLE	EA	.5	W/ITEMS 21,22
28	616251	S3M-PPANH004-40X.250	EA	8.000	W/ITEM 7
31	615513	S1M-PFL1H002-56X.250	EA	6.000	W/ITEM 10
32	615540	S1M-PFL1H004-40X.188	EA	13.000	W/ITEMS 11,12
41	921059	LABEL-CAUTION-STATIC	EA	1.000	W/ITEM 12
42	921148-001	LABEL SET, VXI	EA	1.000	W/ITEMS 21,22
44	921311	LABEL, LOGICAL ADDR, LSB/1	EA	1.000	W/ITEM 11
45	980817	MANUAL, MODEL 7064R, REG BASED	EA	1.000	

Revised 2-15-02

ENGINEERING PARTS LIST

Assembly 407620-210 Low Level Code 02
Description 7064R-210, 2S REG BASED PROTO-N Revision Date 2000-11-16
EA Revision E

#	Component	Description	UM	Qty Reqd	Txt
	SP-152-CA	1260 CARD PAK	EA	1.000	
7	405123	PCB ASSY, REG BASED PROTOTYPE	EA	1.000	
10	456597-001	COVER, TOP, 7064, 2-SLOT, 2-PCB	EA	1.000	
11	456598-001	COVER, BOT, 7064, 2-SLOT, 2-PCB	EA	1.000	
12	456599-001	PANEL, FRT, 7064, 2-SLOT, 2-PCB	EA	1.000	
21	611264	HANDLE-EXT-BOT	EA	2.000	
22	611265	HANDLE-EXT-TOP	EA	2.000	
23	611266	MOUNTING HDW, HANDLE	EA	1.000	W/ITEMS 21,22
25	611441	STN-M/F04M1.18L.187HF.250M	EA	8.000	W/ITEM 11
28	616251	S3M-PPANH004-40X.250	EA	8.000	W/ITEM 7
31	615513	S1M-PFL1H002-56X.250	EA	6.000	W/ITEM 12
32	615540	S1M-PFL1H004-40X.188	EA	15.000	W/ITEMS 10,11
37	921279	LOCQUIC, PRIMER T	EA		W/ITEM 25
38	921280	LOCTITE, 271	EA		W/ITEM 25
41	921059	LABEL-CAUTION-STATIC	EA	1.000	W/ITEM 10
42	921148-001	LABEL SET, VXI	EA	1.000	W/ITEMS 21,22
44	921311	LABEL, LOGICAL ADDR, LSB/1	EA	1.000	W/ITEM 10
45	980817	MANUAL, MODEL 7064R, REG BASED	EA	1.000	

Revised 2-15-02

ENGINEERING PARTS LIST

Assembly 407620-310
Description 7064R-310, 3S REG BASED PROTO-N
EA

Low Level Code 00
Revision Date 1999-03-04
Revision 00000C

#	Component	Description	UM	Qty Reqd	Txt
	SP-152-CA	1260 CARD PAK	EA	1.000	
7	405123	PCB ASSY, REG BASED PROTOTYPE	EA	1.000	
10	456600	COVER, TOP, 7064A, 3-SLOT	EA	1.000	
11	456601	COVER, BOTTOM, 7064A, 3-SLOT	EA	1.000	
12	456602	PANEL, FRONT, 7064M/R, 3-SLOT	EA	1.000	
21	611264	HANDLE-EXT-BOT	EA	1.000	
22	611265	HANDLE-EXT-TOP	EA	1.000	
23	611266	MOUNTING HDW, HANDLE	EA	.500	W/ITEMS 21,22
25	611441	STN-M/F04M1.18L.187HF.250M	EA	8.000	W/ITEM 11
28	616251	S3M-PPANH004-40X.250	EA	8.000	W/ITEM 7
31	615513	S1M-PFL1H002-56X.250	EA	6.000	W/ITEM 12
32	615540	S1M-PFL1H004-40X.188	EA	17.000	W/ITEMS 10,11
37	921279	LOCQUIC, PRIMER T	EA		W/ITEM 25
38	921280	LOCTITE, 271	EA		W/ITEM 25
41	921059	LABEL-CAUTION-STATIC	EA	1.000	W/ITEM 10
42	921148-001	LABEL SET, VXI	EA	1.000	W/ITEMS 21,22
44	921311	LABEL, LOGICAL ADDR, LSB/1	EA	1.000	W/ITEM 10
45	980817	MANUAL, MODEL 7064R, REG BASED	EA	1.000	

Revised 2-15-02

ENGINEERING PARTS LIST

ITEM	REV	PART NO.	DESCRIPTION	QTY	REFERENCE
1		050038	RSCR1-825.000H.12W005	1	R1
2		080116	RSNW2-010.000K16PO8R	5	Z4,Z6,Z8,Z9,Z13
3		110236	CPCH3-0003.3U0016V20	1	C3
4		210118	DISHY-020.0V00.25W	4	D1-D4
5		210120	DILED-002.2V02.OMA	1	D6
6		210121	DILED-002.2V02.OMA	1	D5
7		230786	ICDIG-10H116----RCVR	1	U40
8		230984	ICDIG-74ACT245—TRAN	2	U3,U5
9		231122	ICDIG-74L5641-1	1	U31
10		231126	ICDIG-74538 NAND	1	U19
11		231130	ICDIG-74HCT273—FLOP	1	U17
12		231236	ICDIO-74RCT244—BUFF	5	U16,U18,U21,U23,U42
13		231322	ICDIG-74F32---SOIC	1	U27
14		231380	ICDIG-74ACT04---INV	1	U22
15		231398	ICDIG-74HCT08-AND-SOIC	1	U33
16		231433	ICDIG-74HCT02---SOIC	1	U20
17		231436	ICDIG-74HCTl4---SOIC	1	U32
18		231445	ICDIG-74HCT138—SOIC	1	U30
19		231470	ICDIG-74HCT688—SOIC	2	U14,U29
20		231497	ICLIN-555C SOIC	1	U35
21		231574	ICDIG-74FCT244----SOIC	6	U1,U4,U7-U9,U1 1
22		231575-001	ICPLA-16L8Q-25—PLCCP-U12	1	U12
23		231575-002	ICPLA-16L8Q-25—PLCCP-U15	1	U15
24		231575-003	ICPLA- 1 6L8Q-25--PLCCP-U24	1	U24
25		231575-004	ICPLA- 1 6L8Q-25--PLCCP-U28	1	U28
26		231576-001	ICPLA-22V10H-25-PLCCP-U25	1	U25
27		231576-002	ICPLA-22v10H-25-PLCCP-U26	1	U26
28		231570	ICDIG-74FCT652T-SOIC	4	U2,U6,U10,U13
29		231571	ICDIG-10H123-DRVR	1	U38
30		310193	CKF1-5H005.00U10.1	1	L2
31		415123	PCB,REGBSDPROTOTYPE	1	
32		435123	SCHEMATIC,REG BSD PROTO	REF	
33		601197	POST-ThST-.025 SQ---	2	TPI,TP2
34		601675	CON-PCB-PLG96SD.100T	2	P1,P2
35		601699	SWITCH-DIP-8 POS	1	51
36		601859	SWITCH,DIP 4 POS	1	S6
37		921125	FUSE-05.000A-125V	1	
38		921134	FUSE-10.000-125V	2	F1,F6
39		921232	FUSE,SUB-MINI,2 AMP	4	F2-FS
40		921505	BEAD,FERRITE,LEADED	7	LI,L3-L8
41		R-20-5783	RSCH 1- 150.00H. 12W005	2	R100,R101
42		R-20-5784	RSCH1-180.00H.12W005	2	R23,R25
43		R-20-5786	RSCH1-270.00H.12W005	2	R22,R24
44		R-20-5792	RSCR2-001.00K.12W005	2	R10,R12
45		R-20-5799	RSCH2-004.70K.12W005	47	R2,R3,RS,R7,R11,R14
46					R30-R40,R42-R65
47		R-20-5813	RSCR2-100.00K.12W005	1	R21
48		R-21-1801	CPCH2-0010.0N0050V20	27	C1-C2,C4-C15,C17,C18,C20-C30
49		R-21-1802	CPCR2-0100.0N0050V20	2	C16,C19

RACAL Instruments Inc., 4 Goodyear St. Irvine CA 92718

DOCUMENT TITLE	SIZE	CODE NO.	DOCUMENT NO.	REV
PCB ASSY, REG BASED PROTOTYPE	A	21793	405123	B
	DRN		SHEET 1 of 1	

ENGINEERING PARTS LIST

ITEM	REV	PART NO.	DESCRIPTION	QTY	REFERENCE
1		405123-119	7064R-119, Bare Bd Prototype	1	
2		980817	Manual, Model 7064R, Reg Based	1	

RACAL Instruments Inc., 4 Goodyear St. Irvine CA 92718

DOCUMENT TITLE	SIZE	CODE NO.	DOCUMENT NO.	REV
7064A-119, REG BASED BARE BRD	A	21793	407620-119	B
	DRN		SHEET 1 of 1	

ENGINEERING PARTS LIST

ITEM	REV	PART NO.	DESCRIPTION	QTY	REFERENCE
1		110236	CPCH3-0003.3U0016V20	1	C3
2		R-21 1801	CPCH2-0010.0N0050V20	14	C1-C2,C4-C5
3					
4		310193	CKF1-SH005.00U10.1	1	L2
5		921505	BEAD,FERRITE,LEADED	7	L1,L3-L8
6					
7					
8		415123	PCB,REG BSD PROTOTYPE	1	
9		435123	SCHEMATIC,REG BSD PROTO	REF	
10					
11		601675	CON-PCB-PLG96SD.100T	2	P1,P2
12					
13		921125	FUSE-05.000A-125V	1	F7
14		921134	FUSE-10.000-125V	2	F1,F6
15		921232	FUSE,SUB-MINI,2 AMP	4	F2-F5
16					

RACAL Instruments Inc., 4 Goodyear St. Irvine CA 92718

DOCUMENT TITLE	SIZE	CODE NO.	DOCUMENT NO.	REV
7064R-119, BARE BOARD PROTOTYPE	A	21793	405123-119	B
	DRN		SHEET 1 of 1	

Chapter 6

PRODUCT SUPPORT

Product Support

Racal Instruments has a complete Service and Parts Department. If you need technical assistance or should it be necessary to return your product for repair or calibration, call 1-800-722-3262 or 949-859-8999 and ask for Customer Support. You may also contact Customer Support via E-Mail at:

helpdesk@racalate.com

If parts are required to repair the product at your facility, call 1-800-722-3262 or 1-949-859-8999 and ask for the Parts Department.

When sending your instrument in for repair, complete the form in the back of this manual

Reshipment Instructions

Use the original packing material when returning the switching module to Racal Instruments for calibration or servicing. The original shipping carton and internal packing will provide the necessary support for safe reshipment.

If the original packing material is unavailable, wrap the switching module in ESD barrier material and use foam to surround and protect the instrument.

Re-ship in either the original or a new shipping carton.

Support Offices

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4 Goodyear St., Irvine, CA 92618-2002
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Racal Systems Electronique S.A.
18 Avenue Dutartre, 78150 LeChesnay, France
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Racal Systems Elettronica s.r.l.
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Racal Elektronik System GmbH.
Technologiepark Bergisch Gladbach, Friedrich-Ebert-Strasse,
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Tel.: +49 2204 8442 00; FAX: +49 2204 8442 19

Racal Instruments, Ltd.
Unit 5, 25F., Mega Trade Center, No 1, Mei Wan Road, Tsuen Wan, Hong Kong, PRC

Tel: +852 2405 5500, FAX: +852 2416 4335